

■ Features, Benefits and Applications

- Any frequency between 1 and 80 MHz with 6 decimal places of accuracy
- 100% compatible with and direct replacement of quartz based VCXO
- Widest pull range: ± 25 , ± 50 , ± 100 , ± 200 , ± 400 , ± 800 , ± 1600 PPM
- Superior pull range linearity of $\leq 1\%$, 5x better than quartz's typical linearity of 5%-10%
- LVCMOS/LVTTL compatible output
- Typical tuning voltage: 0 to Vdd
- Two industry-standard 6-pin packages: 5.0 x 3.2, 7.0 x 5.0 mm
- Outstanding silicon reliability of 2 FIT (10x improvement over quartz-based devices)
- Ultra short lead time
- Ideal for telecom clock synchronization, instrumentation, low bandwidth analog PLL, clock recovery (audio and video), broadband and networking

■ Specifications

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency Range	f	1	–	80	MHz	
Frequency Stability						
Initial tolerance	F_init	10	–	10	MHz	at 25°C
Overall Stability	F_stab	-20	–	+20	PPM	Inclusive of initial tolerance (F_init), operating temperature, rated power, supply voltage change, load change. VC
		-25	–	+25	PPM	
		-50	–	+50	PPM	
Pull Range ^[1,2]	PR	± 25 , ± 50 , ± 100 , ± 200 , ± 400 , ± 800 , ± 1600			PPM	
Upper Control Voltage	VC_U	3	–	3.3	V	Vdd = 3.3 V, Voltage at which maximum deviation is guaranteed.
		2.52	–	2.8	V	Vdd = 2.8 V, Voltage at which maximum deviation is guaranteed.
		2.25	–	2.5	V	Vdd = 2.5 V, Voltage at which maximum deviation is guaranteed.
		1.62	–	1.8	V	Vdd = 1.8 V, Voltage at which maximum deviation is guaranteed.
Lower Control Voltage	VC_L	0	–	0.1	V	Voltage at which maximum deviation is guaranteed.
Linearity	Lin	–	–	1	%	
Frequency Change Polarity	–	Positive slope			–	
Control Voltage Bandwidth(-3dB)	V_BW	–	–	8	kHz	
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage	Vdd	1.71	1.8	1.89	V	
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.97	3.3	3.63	V	
Current Consumption	Idd	–	32	TBD	mA	No load condition, f = 20 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V
		–	31	TBD	mA	No load condition, f = 20 MHz, Vdd = 1.8 V
Standby Current	I_std	–	–	TBD	μA	ST = GND, All Vdd, Output is Weakly Pulled Down
Duty Cycle	DC	45	–	55	%	All Vdds
Rise/Fall Time	Tr, Tf	–	1.0	2.0	ns	Vdd = 1.8, 2.5, 2.8 or 3.3 V, 10% - 90% Vdd level
Output Voltage High	VOH	90	–	–	%Vdd	IOH = TBD
Output Voltage Low	VOL	–	–	10	%Vdd	IOL = TBD
Output Load	Ld	–	–	15	pF	Max frequency and supply voltage. Contact SiTime for higher load
Start-up Time	T_start	–	6	10	ms	
OE Enable/Disable Time	T_oe	–	–	TBD		
Resume Time	T_resume	–	3	TBD	ms	Measured from the time ST pin crosses 50% threshold
RMS Period Jitter	T_jitt	–	2	–	ps	f = 75 MHz, all Vdds
RMS Phase Jitter (random)	T_phj	–	0.6	–	ps	f = 75 MHz, Integration bandwidth = 12kHz to 20MHz, all Vdds
Aging	F_aging	–	± 1	–	PPM	1 st year, 25°C

Notes:

1. Absolute Pull Range (APR) is defined as the guaranteed pull range over temperature and voltage.
2. APR = pull range (PR) - frequency stability (F_stab).

Specifications (Cont.)

Pin Description Tables

Pin #1 Functionality
VIN
0 - Vdd: produces voltage dependent frequency change
Pin #2 Functionality
OE
H or Open ³ : specified frequency output
L: output is high impedance
ST
H or Open: specified frequency output
L: output is low level (weak pull down). Oscillation stops

Pin Map	
Pin	Connection
1	VIN
2	OE/ST
3	GND
4	CLK
5	NC
6	VDD

Absolute Maximum Ratings

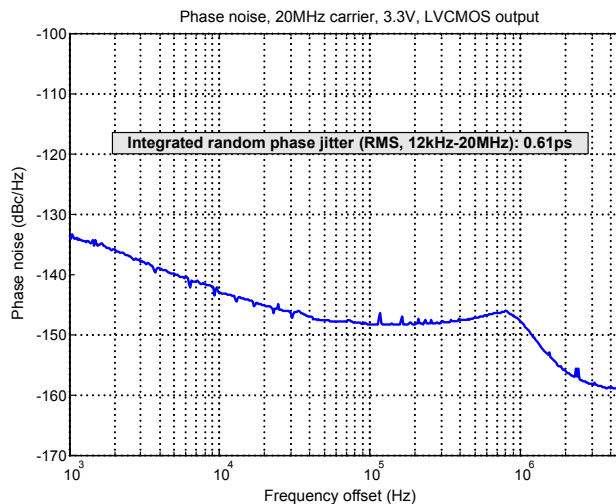
Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge	-	6000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	-	260	°C
Number of Program Writes	-	1	NA
Program Retention over -40 to 125°C, Process, VDD (0 to 3.65 V)	1,000+	-	years

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002; 50kG
Mechanical Vibration	MIL-STD-883F, Method 2007; 70G
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensibility Level	MSL1 @ 260°C

Phase Noise Plot



Note:

3. In 1.8 V mode, a resistor of <100 kΩ between OE pin and VDD is recommended.

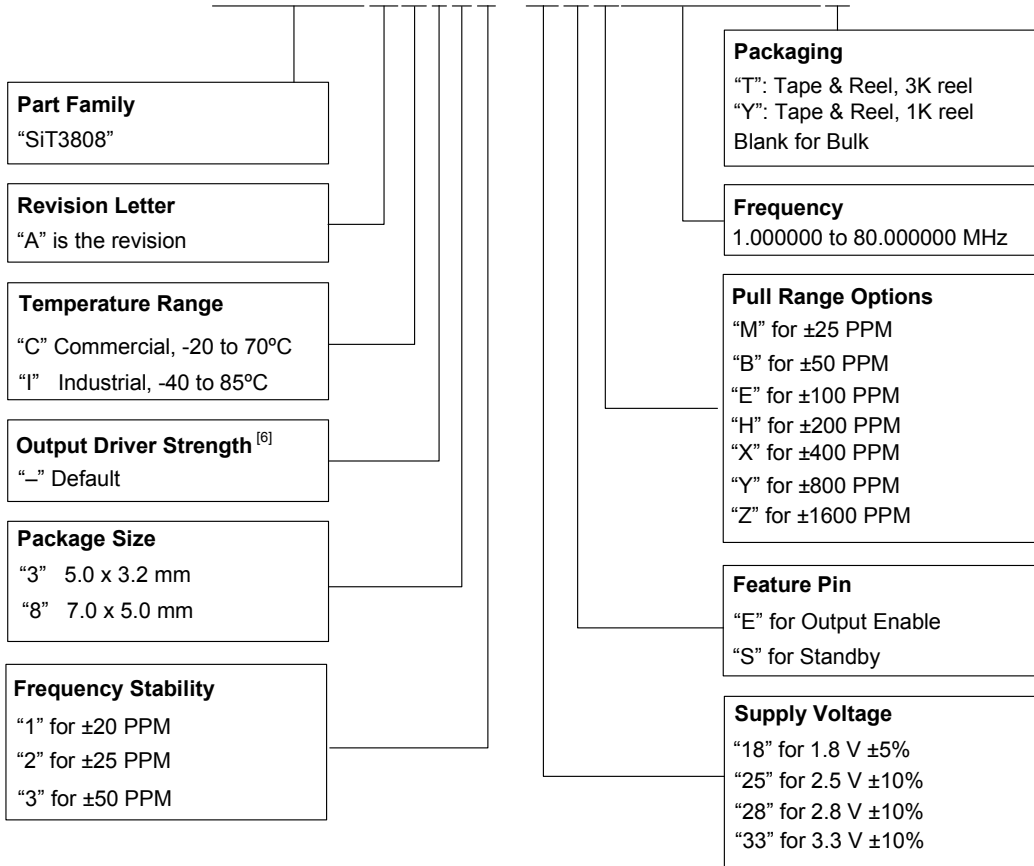
■ Dimensions and Land Patterns

Package Size – Dimensions (Unit: mm) ^[4]	Recommended Land Pattern (Unit: mm) ^[5]
<p>5.0 x 3.2 x 0.75 mm</p>	
<p>7.0 x 5.0 x 0.90 mm</p>	

Notes:

4. Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
5. A capacitor of value 0.1 μ F between Vdd and GND is recommended.

SiT3808AC-31-18SZ75.123456T



Note:

6. Contact SiTime for different drive strength options for driving higher loads or reducing EMI.

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