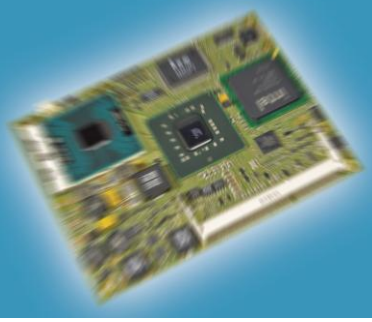


User's Manual

COM Express™

MSC CXC-PV525

Intel® Atom™ D525/D425/N455

COM Express™ Compact Module

Type 2 compliant

Rev. 1.1
March, 2012

Preface

Copyright Notice

Important Information

This documentation is intended for qualified audience only. The product described herein is not an end user product. It was developed and manufactured for further processing by trained personnel.

Disclaimer

Although this document has been generated with the utmost care no warranty or liability for correctness or suitability for any particular purpose is implied. The information in this document is provided “as is” and is subject to change without notice.

EMC Rules

This unit has to be installed in a shielded housing. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her owns expense.

Trademarks

All used product names, logos or trademarks are property of their respective owners.

Certification

MSC Vertriebs GmbH is certified according to DIN EN ISO 9001:2000 standards.

Life-Cycle-Management

MSC products are developed and manufactured according to high quality standards. Our life-cycle-management assures long term availability through permanent product maintenance. Technically necessary changes and improvements are introduced if applicable. A product-change-notification and end-of-life management process assures early information of our customers.

Product Support

MSC engineers and technicians are committed to provide support to our customers whenever needed.
Before contacting Technical Support of MSC Vertriebs GmbH, please consult the respective pages on our web site at www.msc-ge.com/support-boards for the latest documentation, drivers and software downloads.
If the information provided there does not solve your problem, please contact our Technical Support:

Email: support.boards@msc-ge.com
Phone: +49 8165 906-200

Content

1 General Information

1.1 Revision History

Rev.	Date	Description
1.0	28.10.2011	Final Revision
1.1	13.03.2012	Marked the default setup values

1.2 Reference Documents

[1] COM Express Module Base Specification
COM Express Revision 1.0
Last update: July 10th, 2005

[2] PCI Local Bus Specification Rev. 2.1
PCI21.PDF
Last update: June 1st, 1995
http://www.pcisig.com

[3] ATA/ATAPI-6 Specification
d1410r3b.pdf
http://www.t13.org/

[4] Serial ATA Specification
Serial ATA 1.0 gold.pdf
Last update: August 29th, 2002 Rev.1.0
http://www.sata-io.org/

[5] IEEE Std. 802.3-2002
802.3-2002.pdf
http://www.ieee.org

[6] Universal Bus Specification
usb_20.pdf
Last update: April 27th, 2000
http://www.usb.org

1.3 Introduction

COM Express™, an open specification of the PICMG (PCI Industrial Computer Manufacturer Group), is a module concept to bring PCI Express and other latest technologies like SATA, USB 2.0 and LVDS on a COM (Computer On Module).

A COM Express™ module is plugged onto an application-specific base board similar to the ETX concept, but offers more options and a growth path to future CPU technologies. Utilizing different sizes, COM Express™ can be used for highly embedded solutions up to high performance platforms.

The MSC CXC-PV525 is based on Intel® Atom™ CPUs N455, D425 and D525 with the Intel® I/O Controller Hub 8 Mobile (ICH8M).

These Intel® Atom™ CPUs are on the Intel®embedded roadmap of, which means that the processors are available long term.

The CXC-PV525 supports DDR3 memory modules. It provides two 204-pin SO-DIMM sockets providing the flexibility to configure the system up to 4GB of DDR3-DRAM.

The integrated graphics controller contains a refresh of the 3rd generation graphics core. An analog RGB and a single LVDS channel are supported by this GPU.

For evaluation and design-in of the COM Express™ modules we provide evaluation baseboards and develop motherboards providing the interface infrastructure for the COM Express™ module offering PC type connectors for external access.

Up to 440 pins of connectivity are available between COM Express™ modules and the Carrier Board. Legacy buses such as PCI, parallel ATA, LPC, HDA are supported as well as new high speed serial interconnects such as PCI Express, Serial ATA and Gigabit Ethernet.

To enhance interoperability between COM Express™ modules and Carrier Boards, five common signaling configurations (pin-out types) have been defined to ease system integration.

2 Technical Description

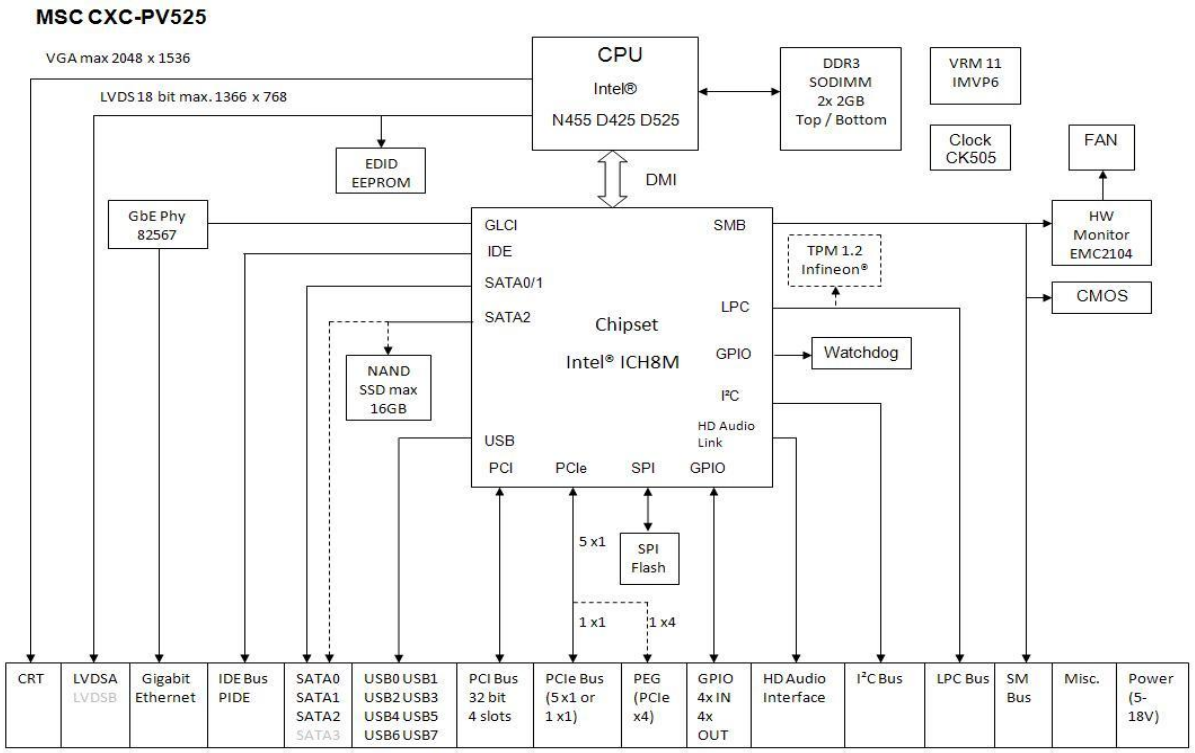
2.1 Key Features

The MSC CXC-PV525 COM Express module is designed as a type 2 module.

Key features include:

- Module size 95 mm x 95 mm
- 18 mm 'z' height with heat-spreader (with 5 mm stack option)
- Dual 220 pin connector (440 pins)
- 2x DDR3 SO-DIMM module
- Eight USB 2.0 ports; four shared over-current lines
- Three Serial ATA ports with data rates up to 3.0Gb/s (300MB/s)
- Five PCI Express x1 lanes
- Support pins for two Express Cards
- One single channel 18-bit LVDS interface
- Analog VGA
- High definition digital audio interface (external codec)
- GBit Ethernet interface
- LPC interface
- Four GPI pins
- Four GPO pins
- +6V to +18V primary power supply input
- +5V standby (optional) and 3.3V RTC power supply inputs
- 32 bit PCI interface
- IDE port (to support legacy ATA devices such as CD-ROM drives and Compact Flash storage cards)
- TPM module (option, TPM 1.2, SLB9635)
- Automatic fan control
- On module SATA NAND flash (option)

2.2 Block diagram



2.3 Com Express Implementation

COM Express™ required and optional features of pin-out type 2 are summarized in the following table. The features identified as minimum (Min.) **shall** be implemented by all modules. Features identified up to maximum (Max) **may** be additionally implemented by a module.

The column MSC CXC-PV525 shows the implemented features of the MSC module:

Function	Type 2	MSC CXC-PV525	Note
	Min / Max		
System I/O			
PCI Express Graphics (PEG)	0 / 1	0	
PCI Express Lanes 0 - 5	1 / 6	5 x1	(Option 1 x4, 1 x1)
PCI Express Lanes 16-31 (same as PEG pins)	0 / 16	0	
SDVO Channels	0 / 2	0	
LVDS Channels	0 / 2	1	1x single channel, 18 bit
VGA Port	0 / 1	1	
TV-Out	NA	0	
PATA Port	1 / 1	1	
SATA Ports	2 / 4	3	(There are only two SATA ports available, when SSD option is used.)
Digital Audio Interface	0 / 1	1	High Definition Audio
USB 2.0 Ports	4 / 8	8	
LAN 0 (10/100Base-T min)	1 / 1	1	82567V Gigabit LAN
PCI Bus - 32 Bit	1 / 1	1	
Express Card Support	1 / 2	2	
LPC Bus	1 / 1	1	
System Management			
General Purpose Inputs	4 / 4	4	
General Purpose Outputs	4 / 4	4	
SMBus	1 / 1	1	
I2C	1 / 1	1	
Watch Dog Timer	0 / 1	1	
Speaker Out	1 / 1	1	
External BIOS ROM support	0 / 1	1	
Reset Functions	1 / 1	1	
Power Management			
Thermal Protection	0 / 1	1	
Battery Low Alarm	0 / 1	1	
Suspend	0 / 1	1	
Wake	0 / 2	2	WOL, PCI Wake
Power Button Support	1 / 1	1	
Power Good	1 / 1	1	
Security			
TPM (on request)	0 / 0	1	TPM 1.2 module

2.4 Functional Units

CPUs	Intel® Atom ™ Processor soldered. D525, 1.8GHz, dual core, 400MHz GPU, DMI D425, 1.8GHz, single core, 400MHz GPU, DMI N455, 1.66GHz, single core, 200MHz GPU, DMI
Chipset	Intel ® 82801GBM ICH8 M
Memory	Two 204-pin DDR3 SO-DIMM sockets for up to 4GB (max. height 1250mil = 31.75mm)
SATA	3 SATA channels up to 300MByte/s each
EIDE	1 Enhanced IDE port ATA/UDMA100
USB	8 x USB 2.0
COM Express™	Type 2 interface, fully compliant
PCI Express™	Five channels PCIe x1
PCI	32 Bit standard interface
LPC	Low Pin Count Bus for heritage interfaces
Graphics	Integrated Graphics Engine DirectX® 9 compliant Pixel Shader 2.0 MPEG2 Hardware Acceleration
Video Memory	Intel® Dynamic Video Memory Technology 4.0
LCD Interface	LVDS 1x18Bit, single channel, max. resolution 1.366 x 768
CRT Interface	max resolution 2.048 x 1.536 @ 60 Hz
Ethernet	10/100/1000Base-TX (Intel® 82567V)
Sound Interface	High Definition Audio interface
Watchdog Timer	PIC12C509A generates reset (programmable, 1s … 255h)
SATA Flash[1]	optional SATA Flash disk, up to 16 GB,
TPM (option)	optional TPM module, TPM 1.2, SLB9635
Fan Supply	3-pin header (12V)
Real Time Clock	integrated in ICH 8 M
EDID-EEPROM	on board EDID EEPROM, enable / disable via SETUP
BIOS	Phoenix BIOS in SPI Flash device
EEPROM	EEPROM for CMOS setup backup
RTC / CMOS	integrated in Intel ® 82801HEM ICH8 M, (typ. 2.7 µA)
Battery	external
System Monitoring	Voltage, Temperature, Fan ▪ Core voltage ▪ 12V (Vin) ▪ CPU thermal diode ▪ Memory temperature sensor ▪ Board temperature sensor ▪ Automatic Fan Control

[1] reduces available SATA channels

2.5 System Memory

The MSC CXC-PV525 CPU module provides two sockets for memory modules which have to meet the following demands:

- 204pin unbuffered DDR3 SO-DIMM
- 1.5V supply voltage
- DDR3-800 / PC3-6400 or faster
- Maximal module height: 30mm
- SPD (Serial Presence Detect) EEPROM

2.6 Power Supply

- **+12V primary power supply input**
- **+5V standby**
  Option, is not required for module operation.
  If not present, customer has to make sure that the supply voltages which are generated on the carrier board are switched off during suspend states, so that no current from the carrier board's signal lines can flow to the CPU board.

- **3.3V RTC power supply**
  Option, is not required for module operation.
  BIOS SETUP data is stored in a non volatile backup memory device (EEPROM), therefore configuration data will not get lost during power off (except for time and date information)

Voltage	Input range	Current
+12V	+6.0V - 18.0 V	See next table
+5V Standby	+4.75V - 5.25 V	max. 2A
+3V RTC power supply	+2.0V - 3.3V	max. 6µA

2.7 Current Dissipation

All measurements were made by plugging a MSC CXC-PV525 module onto a MSC CX-EVA2 Baseboard with a multimeter connected to the +12V Line. The module was equipped with two 1GByte memory modules.

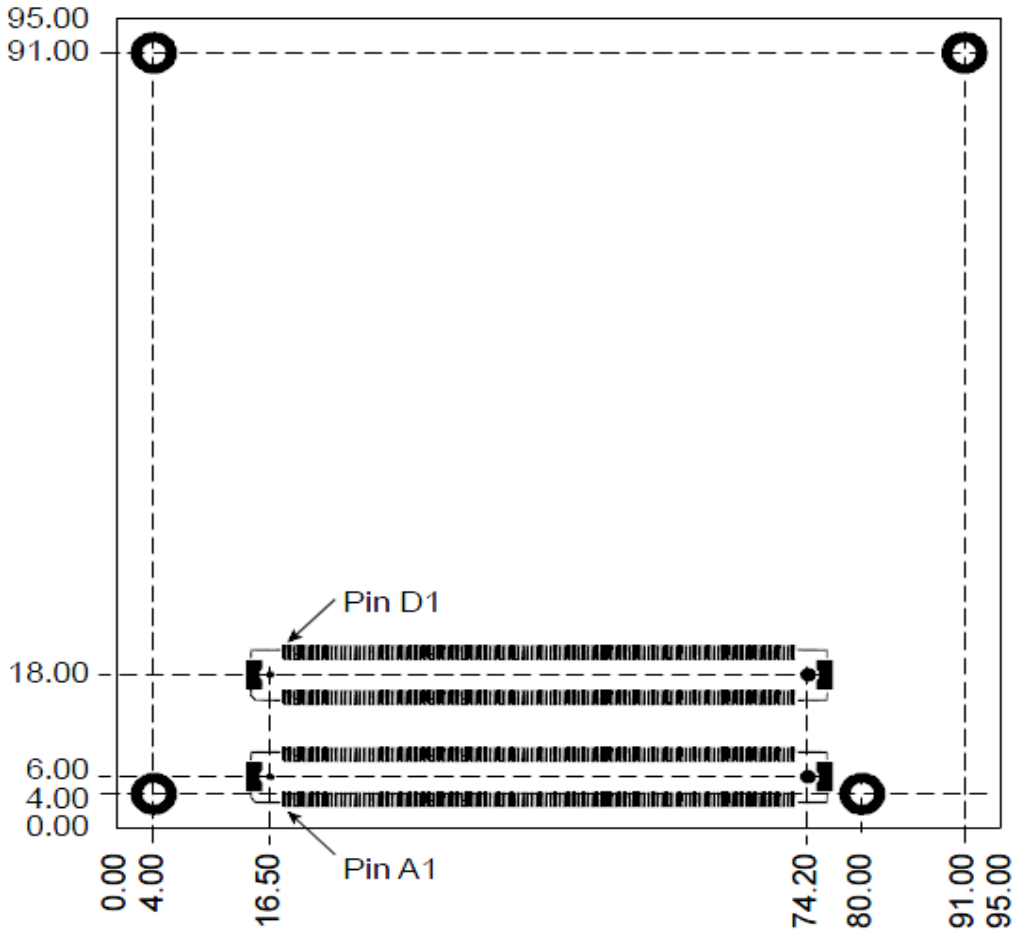
Three tests were performed:

1. Booting Dos 6.22 from an USB stick.
2. Booting Microsoft Windows XP Professional SP3 from an SATA harddrive to the desktop.
3. Booting Microsoft Windows XP Professional SP3 from an SATA harddrive and using BurnIn Test V4.0 to achieve 100% CPU load.

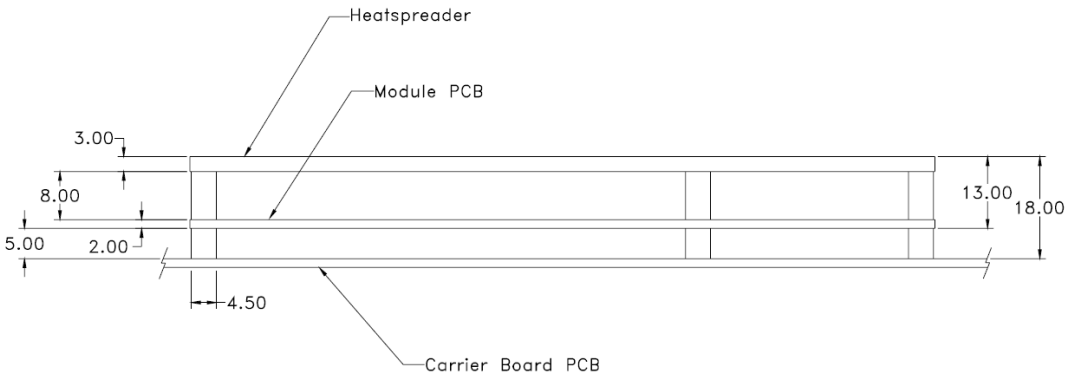
Module (CPU)	DOS Prompt	Windows XP Idle	100% CPU load
Intel® D525	0.86 A (10.3 W)	0.74 A (8.9 W)	1.01 A (12.1 W)
Intel® D425	0.88 A (10.6 W)	0.77 A (9.2 W)	0.90 A (10.8 W)
Intel® N455	0.73 A (8.8 W)	0.59 A (7.1 W)	0.73 A (8.8 W)

2.8 Mechanical Dimensions

2.8.1 Compact module

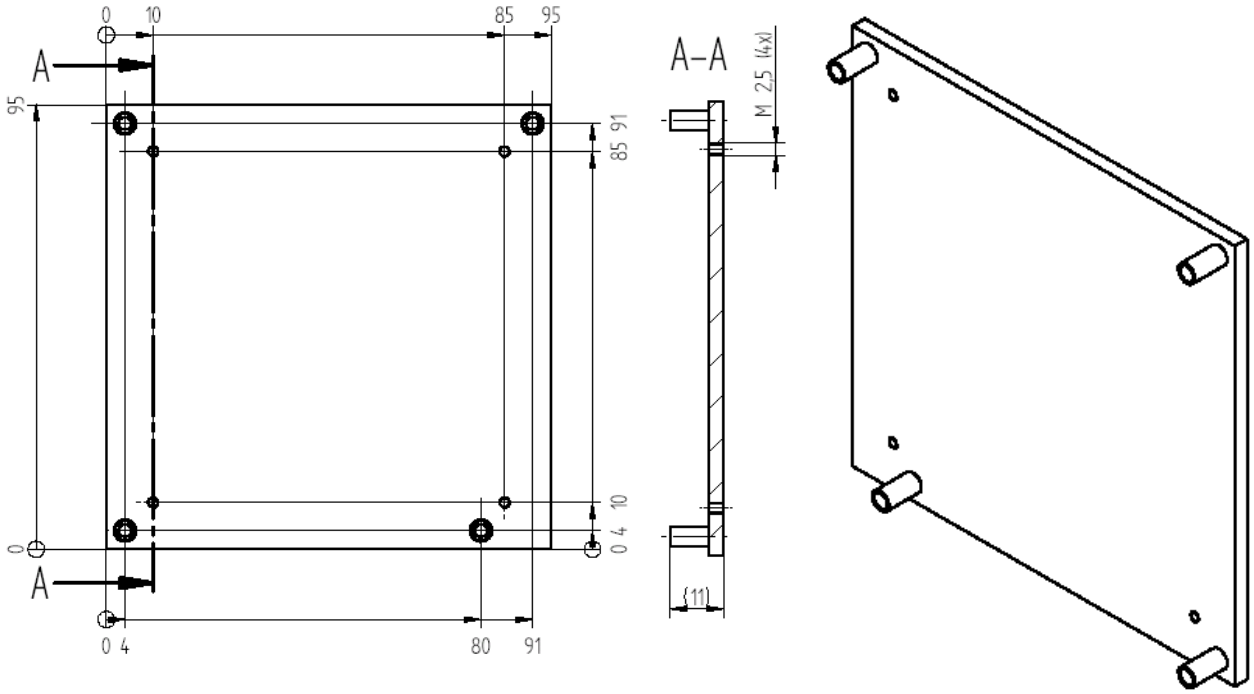


There are two height options defined in the COM Express specification: 5mm and 8mm. The height option is defined by the connectors on the baseboard.



2.9 Thermal specifications

The cooling solution of a COM Express module is based on a heatspreader concept.
A heatspreader is a metal plate (typically aluminium) mounted on the top of the module. The connection between this plate and the module components is typically done by thermal interface materials like phase change foils, gap pads and copper or aluminium blocks. A very good thermal conductivity is required in order to conduct the heat from the cpu and the chipset to the heatspreader plate.
The heatspreader of the MSC module is thermally attached using phase change materials and small aluminium blocks filling the gap between cpu and chipset dies and the heatspreader plate.
The heatspreader is not a heatsink! It is a defined thermal interface for the system designer with fixed mechanical dimensions, so it should be possible to change different module types without problems. There must be a cooling solution for the system. The surface temperature of the heatspreader should not exceed 60°C.
Main issue for the thermal functionality of a system is that each device of the module is operated within its specified thermal values. The max values of CPU and chipset are 100°C, so there may be system implementations where the heatspreader temperature could be higher.
Anyway, in this case it has to be validated that there are no thermal spec violations of any assembled part or integrated circuit over the system temperature range even at worst case conditions.



For mounting instructions and ordering numbers of heatspreaders and complete cooling solutions for this product visit our support pages at http://www.msc-ge.com/support-boards.

2.9.1 Environment

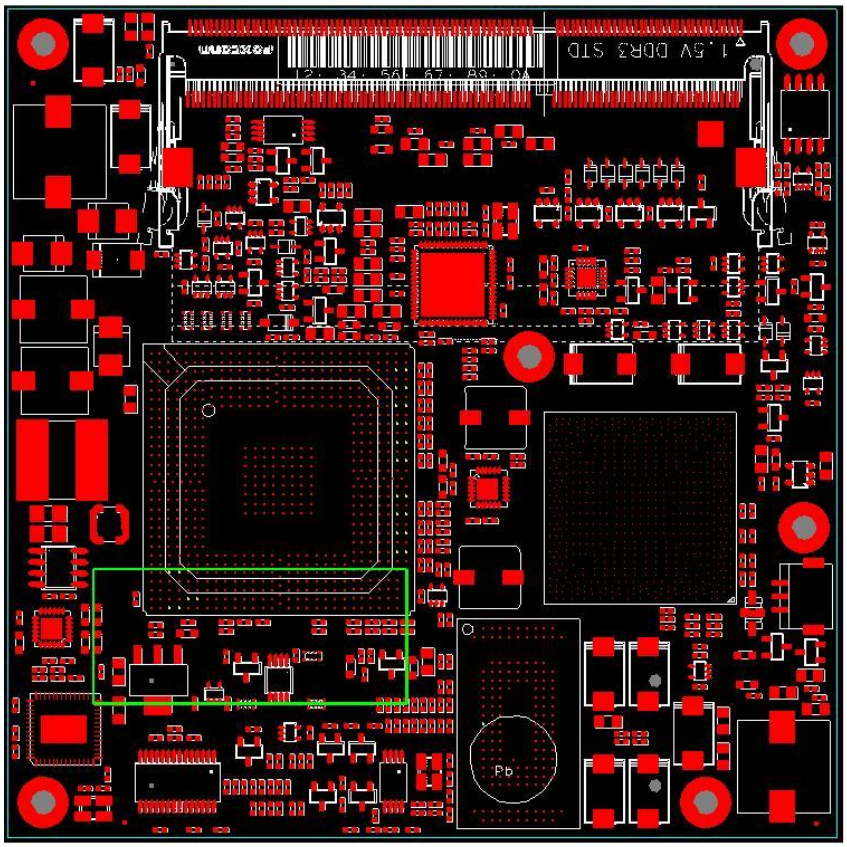
Temperature	0 ... + 60°C (operating), -25 ... + 85°C (non operating)
Humidity (rel.)	5 … 95 % (operating), 5 … 95 % (non operating)

2.10 Installation

2.10.1 Jumpers and switches

There are two jumpers available on the module.

- Clear RTC: By shorting the pins of this jumper, the RTC Clock is reset.
- Recovery: By shorting this jumper, the module forces BIOS recovery function.



2.10.2 Installing a DDR3 SO-DIMM module

The CXC-PV525 board has two standard 204-pin SO-DIMM sockets for 1.5V DDR3-SDRAM SO-DIMM modules.

Using both sockets:

Do not combine different organized memory modules. Always use combinations like 1Rx8 with 1Rx8 or 2Rx8 with 2Rx8.

Note: SO-DIMM Module height should not exceed 1260 mil (= 32 mm)

2.10.3 Optional SATA NAND Flash

An on module SATA NAND Flash up to 16 GB can be assembled connected to one SATA port. There are only two SATA ports left, when SSD option is used.

2.11 Watchdog

The CXC- PV525 board has a watchdog function implemented in a PIC Microcontroller. The watchdog can be enabled and configured in the BIOS Setup.

If the watchdog is enabled a counter is started which generates a reset if it is not retriggered within a programmable time window.

Possible watchdog delays: 1s, 5s, 10s, 30s (default), 1min, 5min, 10min, 30min

Possible watchdog timeout: 0.4s, 1s, 5s, 10s, 30s (default), 1min, 5min, 10min

The time delay starts as soon as it is enabled in the BIOS

MSC provides a software API which gives the application software access to the Watchdog functionality if needed.

2.12 Signal description

Pins are marked in the following tables with the power rail associated with the pin, and, for input and I/O pins, with the input voltage tolerance. The pin power rail and the pin input voltage tolerance **may** be different. For example, the PCI group is defined as having a 3.3V power rail, meaning that the output signals will only be driven to 3.3V, but the pins are tolerant of 5V signals.
An additional label, “Suspend”, indicates that the pin is active during suspend states (S3, S4, S5). If suspend modes are used, then care must be taken to avoid loading signals that are active during suspend to avoid excessive suspend mode current draw.

2.12.1 High Definition Audio

Signal	Pin Type	Signal Level	Power Rail	Power Tolerance	PU/PD	Description	Source / Target
AC_RST#	Output	CMOS	3.3V Sus.	3.3V		Reset output to CODEC, active low.	ICH8M
AC_SYNC	Output	CMOS	3.3V	3.3V	8k2 PU 20k PD	48kHz fixed-rate, sample-synchronization signal to the CODEC(s).	ICH8M
AC_BITCLK	Output	CMOS	3.3V	3.3V	20k PD	24.00 MHz serial data clock generated by the ICH9-M	ICH8M
AC_SDOUT	Output	CMOS	3.3V	3.3V	20k PD	Serial TDM data output to the CODEC.	ICH8M
AC_SDIN[0:2]	Input	CMOS	3.3V Sus.	3.3V	20k PD	Serial TDM data inputs from up to 3 CODECs.	ICH8M

2.12.2 Ethernet

Signal	Pin Type	Signal Level	Power Rail	Power Tolerance	PU/PD	Description	Source / Target
GBE0_MDI[0:3]+ GBE0_MDI[0:3]-	Input/ Output	Analog	3.3V Sus.			Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. MDI[0]+/- B1_DA+/- MDI[1]+/- B1_DB+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	82567V
GBE0_ACT#	Open Drain	CMOS	3.3V Sus.	3.3V		Gigabit Ethernet Controller 0 activity indicator, active low.	82567V
GBE0_LINK#	Open Drain	CMOS	3.3V Sus.	3.3V		Gigabit Ethernet Controller 0 link indicator, active low.	82567V
GBE0_LINK100#	Open Drain	CMOS	3.3V Sus.	3.3V		Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	82567V
GBE0_LINK1000#	Open Drain	CMOS	3.3V Sus.	3.3V		Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	82567V
GBE0_CTREF	REF			GND min 3.3V max		82567 (1000MBit) : 1,8V	82567V

2.12.3 IDE

Signal	Pin Type	Signal Level	Power Rail	Power Tolerance	PU/PD	Description	Source / Target
IDE_D[0:6,8:15]	I/O	CMOS	3.3V	5V		Bidirectional data to / from IDE device.	ICH8M
IDE_D[7]	I/O	CMOS	3.3V	5V	15k PD	Bidirectional data to / from IDE device.	ICH8M
IDE_A[0:2]	O	CMOS	3.3V	3.3V		Address lines to IDE device.	ICH8M
IDE_IOW#	O	CMOS	3.3V	3.3V		I/O write line to IDE device. Data latched on trailing (rising) edge.	ICH8M
IDE_IOR#	O	CMOS	3.3V	3.3V		I/O read line to IDE device.	ICH8M
IDE_REQ	I	CMOS	3.3V	5V	15k PD	IDE Device DMA Request. It is asserted by the IDE device to request a data transfer.	ICH8M
IDE_ACK#	O	CMOS	3.3V	3.3V		IDE Device DMA Acknowledge.	ICH8M
IDE_CS1#	O	CMOS	3.3V	3.3V		IDE Device Chip Select for 1F0h to 1FFh range.	ICH8M
IDE_CS3#	O	CMOS	3.3V	3.3V		IDE Device Chip Select for 3F0h to 3FFh range.	ICH8M
IDE_IORDY	I	CMOS	3.3V	5V	4k7 PU	IDE device I/O ready input. Pulled low by the IDE device to extend the cycle.	ICH8M
IDE_RESET#	O	CMOS	3.3V Sus.	3.3V		Reset output to IDE device, active low.	
IDE_IRQ	I	CMOS	3.3V	5V	8k2 PU	Interrupt request from IDE device.	ICH8M
IDE_CBLID#	I	CMOS	3.3V	3.3V	10k PD	Input from off-module hardware indicating the type of IDE cable being used. High indicates a 40-pin cable used for legacy IDE modes. Low indicates that an 80-pin cable with interleaved grounds is used. Such a cable is required for Ultra-DMA 66, 100 and 133 modes.	ICH8M

2.12.4 Serial ATA

Signal	Pin Type	Signal Level	Power Rail	Remark	PU/PD	Description	Source / Target
SATA0_TX+ SATA0_TX-	O	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 transmit differential pair.	ICH8M
SATA0_RX+ SATA0_RX-	I	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 receive differential pair.	ICH8M
SATA1_TX+ SATA1_TX-	O	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 transmit differential pair.	ICH8M
SATA1_RX+ SATA1_RX-	I	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 receive differential pair.	ICH8M
SATA2_TX+ SATA2_TX-	O	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 transmit differential pair.	ICH8M
SATA2_RX+ SATA2_RX-	I	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 receive differential pair.	ICH8M
SATA3_TX+ SATA3_TX-	O	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 transmit differential pair.	ICH8M
SATA3_RX+ SATA3_RX-	I	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 receive differential pair.	ICH8M
ATA_ACT#	O	CMOS	3.3V	3.3V		SATA activity indicator, active low.	

2.12.5 PCI Express Lanes

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/ PD	Description	Source / Target
PCIE_TX[0:4]+ PCIE_TX[0:4]-	O	PCIe	3.3V	AC coupled on module		PCI Express Differential Transmit Pairs 0 through 4	ICH8M
PCIE_RX[0:4]+ PCIE_RX[0:4]-	I	PCIe	3.3V	AC coupled off module		PCI Express Differential Receive Pairs 0 through 4	ICH8M
PCIE_TX[5]+ PCIE_TX[5]-	O	PCIe	3.3V	AC coupled on module		PCI Express Differential Transmit Pair 5	not supported
PCIE_RX[5]+ PCIE_RX[5]-	I	PCIe	3.3V	AC coupled off module		PCI Express Differential Receive Pair 5	not supported
PCIE_TX[16:31]+ PCIE_TX[16:31]-	O	PCIe	3.3V	AC coupled on module		PCI Express Differential Transmit Pairs 16 through 31. These are same lines as PEG_TX[0:15]+ and - in module pin-out types 4 and 5.	not supported
PCIE_RX[16:31]+ PCIE_RX[16:31]-	I	PCIe	3.3V	AC coupled off module		PCI Express Differential Receive Pairs 16 through 31. These are the same lines as PEG_RX[0:15]+ and - in module pin-out types 4 and 5.	not supported
PCIE_CLK_REF+ PCIE_CLK_REF-	O	PCIe CLK	3.3V	AC coupled on module		Reference clock output for all PCI Express and PCI Express Graphics lanes.	CK505

2.12.6 PCI Express Lanes x16

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
PEG_TX[0:15]+ PEG_TX[0:15]-	O	PCIe	3.3V	AC coupled on module		PCI Express Graphics transmit differential pairs. Some of these are multiplexed with SDVO lines (see SDVO section). These are the same lines as PCIE_TX[16:31]+ and - in module pin-out types 4 and 5.	not supported
PEG_RX[0:15]+ PEG_RX[0:15]-	I	PCIe	3.3V	AC coupled off module		PCI Express Graphics receive differential pairs. Some of these are multiplexed with SDVO lines (see SDVO section). These are the same lines as PCIE_RX[16:31]+ and - in module pin-out types 4 and 5.	not supported
PEG_LANE_RV#	I	CMOS	3.3V	3.3V	5k7 PU	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order. Be aware that the SDVO lines that share this interface do not necessarily reverse order if this strap is low.	not supported
PEG_ENABLE#	I	CMOS	3.3V	3.3V	100k PU	Strap to enable PCI Express x16 external graphics interface. Pull low to disable internal graphics and enable the x16 interface.	not supported

2.12.7 Express Card Support

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
EXCD[0]_CPPE#	I	CMOS	3.3V	3.3V	8k2 PU	ExpressCard card request, active low	ICH8M
EXCD[1]_CPPE#	I	CMOS	3.3V	3.3V		ExpressCard card request, active low	not supported
EXCD[0]_RST#	O	CMOS	3.3V	3.3V	8k2 PU	ExpressCard reset, active low	ICH8M
EXCD[1]_RST#	O	CMOS	3.3V	3.3V	8k2 PU	ExpressCard reset, active low	ICH8M

2.12.8 PCI Bus

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
PCI_AD[0:31]	I/O	CMOS	3.3V	5V		PCI bus multiplexed address and data lines	ICH8M
PCI_C/BE[0:3]#	I/O	CMOS	3.3V	5V		PCI bus byte enable lines, active low	ICH8M
PCI_DEVSEL#	I/O	CMOS	3.3V	5V	8k2 PU	PCI bus Device Select, active low.	ICH8M
PCI_FRAME#	I/O	CMOS	3.3V	5V	8k2 PU	PCI bus Frame control line, active low.	ICH8M
PCI_IRDY#	I/O	CMOS	3.3V	5V	8k2 PU	PCI bus Initiator Ready control line, active low.	ICH8M
PCI_TRDY#	I/O	CMOS	3.3V	5V	8k2 PU	PCI bus Target Ready control line, active low.	ICH8M
PCI_STOP#	I/O	CMOS	3.3V	5V	8k2 PU	PCI bus STOP control line, active low, driven by cycle initiator.	ICH8M
PCI_PAR	I/O	CMOS	3.3V	5V		PCI bus parity	ICH8M
PCI_PERR#	I/O	CMOS	3.3V	5V	8k2 PU	Parity Error: An external PCI device drives PERR# when it receives data that has a parity error.	ICH8M
PCI_REQ[0:3]#	I	CMOS	3.3V	5V	8k2 PU	PCI bus master request input lines, active low.	ICH8M
PCI_GNT[0:3]#	O	CMOS	3.3V	5V		PCI bus master grant output lines, active low.	ICH8M
PCI_RESET#	O	CMOS	3.3V Sus.	5V		PCI Reset output, active low.	ICH8M
PCI_LOCK#	I/O	CMOS	3.3V	5V	8k2 PU	PCI Lock control line, active low.	ICH8M
PCI_SERR#	I/O OD	CMOS	3.3V	5V	8k2 PU	System Error: SERR# may be pulsed active by any PCI device that detects a system error condition.	ICH8M
PCI_PME#	I	CMOS	3.3V Sus.	3.3V	20k PU	PCI Power Management Event: PCI peripherals drive PME# to wake system from low-power states S1–S5.	ICH8M
PCI_CLKRUN#	I/O	CMOS	3.3V	3.3V	10k PU	Bidirectional pin used to support PCI clock run protocol for mobile systems.	ICH8M
PCI_IRQ[A:D]#	I	CMOS	3.3V	5V	8k2 PU	PCI interrupt request lines.	ICH8M
PCI_CLK	O	CMOS	3.3V	3.3V		PCI 33MHz clock output.	CK505
PCI_M66EN	I	CMOS	3.3V	5V		Module input signal indicates whether an off-module PCI device is capable of 66MHz operation. Pulled to GND by Carrier Board device or by Slot Card if the devices are NOT capable of 66 MHz operation. If the module is not capable of supporting 66 MHz PCI operation, this input may be a no-connect on the module. If the module is capable of supporting 66 MHz PCI operation, and if this input is held low by the Carrier Board, the module PCI interface shall operate at 33 MHz.	Not supported

2.12.9 USB

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/ PD	Description	Source / Target
USB[0:7]+ USB[0:7]-	I/O	USB	3.3V Sus.	3.3V	15k PD	USB differential pairs, channels 0 through 7	ICH8M
USB_0_1_OC#	I	CMOS	3.3V Sus.	3.3V	8k2 PU	USB over-current sense, USB channels 0 and 1. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	ICH8M
USB_2_3_OC#	I	CMOS	3.3V Sus.	3.3V	8k2 PU	USB over-current sense, USB channels 2 and 3. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	ICH8M
USB_4_5_OC#	I	CMOS	3.3V Sus.	3.3V	8k2 PU	USB over-current sense, USB channels 4 and 5. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	ICH8M
USB_6_7_OC#	I	CMOS	3.3V Sus.	3.3V	8k2 PU	USB over-current sense, USB channels 6 and 7. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	ICH8M

2.12.10 LVDS Flat Panel

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
LVDS_A[0:3]+ LVDS_A[0:3]-	O	LVDS				LVDS Channel A differential pairs	CPU
LVDS_A_CK+ LVDS_A_CK-	O	LVDS				LVDS Channel A differential clock	CPU
LVDS_VDD_EN	O	CMOS	3.3V	3.3V	100k PD	LVDS panel power enable	CPU
LVDS_BKLT_EN	O	CMOS	3.3V	3.3V	100k PD	LVDS panel backlight enable	CPU
LVDS_BKLT_CTRL	O	CMOS	3.3V	3.3V	100k PD	LVDS panel backlight brightness control	CPU
LVDS_I2C_CK	O	CMOS	3.3V	3.3V	8k2 PU	I2C clock output for LVDS display use	CPU
LVDS_I2C_DAT	I/O OD	CMOS	3.3V	3.3V	8k2 PU	I2C data line for LVDS display use	CPU

2.12.11 LPC Bus

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
LPC_AD[0:3]	I/O	CMOS	3.3V	3.3V		LPC multiplexed address, command and data bus	ICH8M
LPC_FRAME#	O	CMOS	3.3V	3.3V		LPC frame indicates the start of an LPC cycle	ICH8M
LPC_DRQ[0:1]#	I	CMOS	3.3V	3.3V	20k PU	LPC serial DMA request	ICH8M
LPC_SERIRQ	I/O	CMOS	3.3V	3.3V		LPC serial interrupt	ICH8M
LPC_CLK	O	CMOS	3.3V	3.3V		LPC clock output - 33MHz nominal	CK505

2.12.12 Analog VGA

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
VGA_RED	O	Analog			150R PD	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	CPU
VGA_GRN	O	Analog			150R PD	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	CPU
VGA_BLU	O	Analog			150R PD	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	CPU
VGA_HSYNC	O	CMOS	3.3V	3.3V		Horizontal sync output to VGA monitor	CPU
VGA_VSYNC	O	CMOS	3.3V	3.3V		Vertical sync output to VGA monitor	CPU
VGA_I2C_CK	O	CMOS	3.3V	3.3V	2k2 PU	DDC clock line (I2C port dedicated to identify VGA monitor capabilities)	CPU
VGA_I2C_DAT	I/O OD	CMOS	3.3V	3.3V	2k2 PU	DDC data line.	CPU

2.12.13 SPI Interface

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
SPI_CS#	O	CMOS	3.3V Sus.	3.3V		Chip select for Carrier board SPI	ICH8M
SPI_MISO	I	CMOS	3.3V Sus.	3.3V	8k2 PU	Data in to module from Carrier SPI	ICH8M
SPI_MOSI	O	CMOS	3.3V Sus.	3.3V	8k2 PU	Data out from module to Carrier SPI	ICH8M
SPI_CLK	O	CMOS	3.3V Sus.	3.3V		Clock from module to Carrier SPI	ICH8M
SPI_POWER	O		3.3V Sus.	3.3V		Power supply for Carrier Board SPI	
BIOS_DIS0#	I	CMOS	3.3V Sus.	3.3V	4k7 PU	Selection strap to determine the BIOS boot device Boot BIOS destination select 0 - LPC/FWH 1 - SPI	ICH8M
BIOS_DIS1#	I	CMOS	3.3V Sus.	3.3V		Selection strap to determine the BIOS boot device	Not supported

2.12.14 Miscellaneous

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
I2C_CK	O	CMOS	3.3V	3.3V	2k2 PU	General purpose I2C port clock output	ICH8M
I2C_DAT	I/O	CMOS	3.3V	3.3V	2k2 PU	General purpose I2C port data I/O line	ICH8M
SPKR	O	CMOS	3.3V	3.3V	20k PD	Output for audio enunciator - the "speaker" in PC-AT systems	ICH8M
BIOS_DISABLE#	I	CMOS	3.3V Sus.	3.3V	4k7 PU	Module BIOS disable input. Pull low to disable module BIOS.	Disables SPI Flash
WDT	O	CMOS	3.3V	3.3V	10k PU	Output indicating that a watchdog time-out event has occurred.	PIC12C509
KBD_RST#	I	CMOS	3.3V	3.3V	10k PU	Input to module from (optional) external keyboard controller that can force a reset. Pulled high on the module. This is a legacy artifact of the PC-AT.	ICH8M
KBD_A20GATE		CMOS	3.3V	3.3V	10k PU	Input to module from (optional) external keyboard controller that can be used to control the CPU A20 gate line. The A20GATE restricts the memory access to the bottom megabyte and is a legacy artifact of the PC- AT. Pulled high on the module.	ICH8M

2.12.15 Power and System Management

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
PWRBTN#	I	CMOS	3.3V Sus.	3.3V	10k PU	Power button to bring system out of Suspend states, active on falling edge.	ICH8M
SYS_RESET#	I	CMOS	3.3V Sus.	3.3V	10k PU	Reset button input. Active low input. System is held in hardware reset while this input is low, and comes out of reset upon release.	ICH8M
CB_RESET#	O	CMOS	3.3V Sus.	3.3V		Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	ICH8M
PWR_OK	I	CMOS	3.3V Sus.	3.3V	220k PU	Power OK from main power supply. A high value indicates that the power is good.	Power Good logic
SUS_STAT#	O	CMOS	3.3V Sus.	3.3V		Indicates imminent suspend operation; used to notify LPC devices.	ICH8M
SUS_S3#	O	CMOS	3.3V Sus.	3.3V		Indicates system is in Suspend to RAM state. Active low output.	ICH8M
SUS_S4#	O	CMOS	3.3V Sus.	3.3V		Indicates system is in Suspend to Disk state. Active low output.	ICH8M
SUS_S5#	O	CMOS	3.3V Sus.	3.3V		Indicates system is in Soft Off state. Also known as "PS_ON" and can be used to control an ATX power supply.	ICH8M
WAKE0#	I	CMOS	3.3V Sus.	3.3V	1k PU	PCI Express wake up signal.	ICH8M
WAKE1#	I	CMOS	3.3V Sus.	3.3V	1k PU	General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.	ICH8M
BATLOW#	I	CMOS	3.3V Sus.	3.3V	10k PU	Indicates that external battery is low.	ICH8M
THRM#	I	CMOS	3.3V Sus.	3.3V	10k PU	Input from off-module temp sensor indicating an over-temp situation.	ICH8M
THERMTRIP#	O	CMOS	3.3V	3.3V	330R PU	Active low output indicating that the CPU has entered thermal shutdown.	CPU
SMB_CK	I/O OD	CMOS	3.3V Sus.	3.3V	Act. PU	System Management Bus bidirectional clock line. Power sourced through 5V standby rail and main power rails.	ICH8M
SMB_DAT	I/O OD	CMOS	3.3V Sus.	3.3V	Act. PU	System Management Bus bidirectional data line. Power sourced through 5V standby rail and main power rails.	ICH8M
SMB_ALERT#	I	CMOS	3.3V Sus.	3.3V	10k PU	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 5V standby rail and main power rails.	ICH8M

2.12.16 General Purpose I/O

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
GPO[1..2]	O	CMOS	3.3V	3.3V		General purpose output pins.	ICH8M
GPO0	O	CMOS	3.3V	3.3V	10k PD	General purpose output pins.	ICH8M
GPO3	O	CMOS	3.3V	3.3V	10k PD	General purpose output pins.	ICH8M
GPI[0:3]	I	CMOS	3.3V	3.3V		General purpose input pins.	ICH8M

2.12.17 Module Type Definition

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
TYPE[0:2]#	Type Detect					The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) 22 rare no-connects (NC). For Pin-out Type 1, these pins are don't care (X). TYPE2# TYPE1# TYPE0# X X X Pin-out Type 1 **NC NC NC Pin-out Type 2** NC NC GND Pin-out Type 3 (no IDE) NC GND NC Pin-out Type 4 (no PCI) NC GND GND Pin-out Type 5 (no IDE, no PCI) The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as a LED.	For this Type 2 board, all Type Detect pins are n.c.

2.12.18 Power and GND

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
VCC_12V	Power		12V (±5%)			Primary power input: +6V - +18V	Voltage Regulators
VCC_5V_SBY	Power		5V (±5%)			Standby power input: +5.0V (±5%) If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	VCC3.3V SUS regulator
VCC_RTC	Power					Real-time clock circuit-power input : +3.0V (+2.0V to +3.3V)	ICH8M
GND	Power					Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	

2.13 Pin List for MSC CXC-PV525 module (Type 2)

Row A		Row B		Row C		Row D	
A1	GND (FIXED)	B1	GND (FIXED)	C1	GND (FIXED)	D1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	C2	IDE_D7	D2	IDE_D5
A3	GBE0_MDI3+	B3	LPC_FRAME#	C3	IDE_D6	D3	IDE_D10
A4	GBE0_LINK100#	B4	LPC_AD0	C4	IDE_D3	D4	IDE_D11
A5	GBE0_LINK1000#	B5	LPC_AD1	C5	IDE_D15	D5	IDE_D12
A6	GBE0_MDI2-	B6	LPC_AD2	C6	IDE_D8	D6	IDE_D4
A7	GBE0_MDI2+	B7	LPC_AD3	C7	IDE_D9	D7	IDE_D0
A8	GBE0_LINK#	B8	LPC_DRQ0#	C8	IDE_D2	D8	IDE_REQ
A9	GBE0_MDI1-	B9	LPC_DRQ1#	C9	IDE_D13	D9	IDE_IOW#
A10	GBE0_MDI1+	B10	LPC_CLK	C10	IDE_D1	D10	IDE_ACK#
A11	GND (FIXED)	B11	GND (FIXED)	C11	GND (FIXED)	D11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	C12	IDE_D14	D12	IDE_IRQ
A13	GBE0_MDI0+	B13	SMB_CK	C13	IDE_IORDY	D13	IDE_A0
A14	GBE0_CTREF	B14	SMB_DAT	C14	IDE_IOR#	D14	IDE_A1
A15	SUS_S3#	B15	SMB_ALERT#	C15	PCI_PME#	D15	IDE_A2
A16	SATA0_TX+	B16	SATA1_TX+	C16	PCI_GNT2#	D16	IDE_CS1#
A17	SATA0_TX-	B17	SATA1_TX-	C17	PCI_REQ2#	D17	IDE_CS3#
A18	SUS_S4#	B18	SUS_STAT#	C18	PCI_GNT1#	D18	IDE_RESET#
A19	SATA0_RX+	B19	SATA1_RX+	C19	PCI_REQ1#	D19	PCI_GNT3#
A20	SATA0_RX-	B20	SATA1_RX-	C20	PCI_GNT0#	D20	PCI_REQ3#
A21	GND (FIXED)	B21	GND (FIXED)	C21	GND (FIXED)	D21	GND (FIXED)
A22	SATA2_TX+	B22	SATA3_TX+	C22	PCI_REQ0#	D22	PCI_AD1
A23	SATA2_TX-	B23	SATA3_TX-	C23	PCI_RESET#	D23	PCI_AD3
A24	SUS_S5#	B24	PWR_OK	C24	PCI_AD0	D24	PCI_AD5
A25	SATA2_RX+	B25	SATA3_RX+	C25	PCI_AD2	D25	PCI_AD7
A26	SATA2_RX-	B26	SATA3_RX-	C26	PCI_AD4	D26	PCI_C/BE0#
A27	BATLOW#	B27	WDT	C27	PCI_AD6	D27	PCI_AD9
A28	ATA_ACT#	B28	AC_SDIN2	C28	PCI_AD8	D28	PCI_AD11
A29	AC_SYNC	B29	AC_SDIN1	C29	PCI_AD10	D29	PCI_AD13
A30	AC_RST#	B30	AC_SDIN0	C30	PCI_AD12	D30	PCI_AD15
A31	GND (FIXED)	B31	GND (FIXED)	C31	GND (FIXED)	D31	GND (FIXED)
A32	AC_BITCLK	B32	SPKR	C32	PCI_AD14	D32	PCI_PAR
A33	AC_SDOUT	B33	I2C_CK	C33	PCI_C/BE1#	D33	PCI_SERR#
A34	BIOS_DIS0#	B34	I2C_DAT	C34	PCI_PERR#	D34	PCI_STOP#
A35	THRMTRIP#	B35	THRM#	C35	PCI_LOCK#	D35	PCI_TRDY#
A36	USB6-	B36	USB7-	C36	PCI_DEVSEL#	D36	PCI_FRAME#
A37	USB6+	B37	USB7+	C37	PCI_IRDY#	D37	PCI_AD16
A38	USB_6_7_OC#	B38	USB_4_5_OC#	C38	PCI_C/BE2#	D38	PCI_AD18
A39	USB4-	B39	USB5-	C39	PCI_AD17	D39	PCI_AD20
A40	USB4+	B40	USB5+	C40	PCI_AD19	D40	PCI_AD22
A41	GND (FIXED)	B41	GND (FIXED)	C41	GND (FIXED)	D41	GND (FIXED)
A42	USB2-	B42	USB3-	C42	PCI_AD21	D42	PCI_AD24
A43	USB2+	B43	USB3+	C43	PCI_AD23	D43	PCI_AD26
A44	USB_2_3_OC#	B44	USB_0_1_OC#	C44	PCI_C/BE3#	D44	PCI_AD28
A45	USB0-	B45	USB1-	C45	PCI_AD25	D45	PCI_AD30
A46	USB0+	B46	USB1+	C46	PCI_AD27	D46	PCI_IRQC#
A47	VCC_RTC	B47	EXCD1_PERST#	C47	PCI_AD29	D47	PCI_IRQD#
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	C48	PCI_AD31	D48	PCI_CLKRUN#
A49	EXCD0_CPPE#	B49	SYS_RESET#	C49	PCI_IRQA#	D49	PCI_M66EN
A50	LPC_SERIRQ	B50	CB_RESET#	C50	PCI_IRQB#	D50	PCI_CLK

	= not supported on MSC CXC-PV525 module

Row A		Row B		Row C		Row D	
A51	GND (FIXED)	B51	GND (FIXED)	C51	GND (FIXED)	D51	GND (FIXED)
A52	PCIE_TX5+	B52	PCIE_RX5+	C52	PEG_RX0+	D52	PEG_TX0+
A53	PCIE_TX5-	B53	PCIE_RX5-	C53	PEG_RX0-	D53	PEG_TX0-
A54	GPI0	B54	GPO1	C54	TYPE0#	D54	PEG_LANE_RV#
A55	PCIE_TX4+	B55	PCIE_RX4+	C55	PEG_RX1+	D55	PEG_TX1+
A56	PCIE_TX4-	B56	PCIE_RX4-	C56	PEG_RX1-	D56	PEG_TX1-
A57	GND	B57	GPO2	C57	TYPE1#	D57	TYPE2#
A58	PCIE_TX3+	B58	PCIE_RX3+	C58	PEG_RX2+	D58	PEG_TX2+
A59	PCIE_TX3-	B59	PCIE_RX3-	C59	PEG_RX2-	D59	PEG_TX2-
A60	GND (FIXED)	B60	GND (FIXED)	C60	GND (FIXED)	D60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+	C61	PEG_RX3+	D61	PEG_TX3+
A62	PCIE_TX2-	B62	PCIE_RX2-	C62	PEG_RX3-	D62	PEG_TX3-
A63	GPI1	B63	GPO3	C63	RSVD	D63	RSVD
A64	PCIE_TX1+	B64	PCIE_RX1+	C64	RSVD	D64	RSVD
A65	PCIE_TX1-	B65	PCIE_RX1-	C65	PEG_RX4+	D65	PEG_TX4+
A66	GND	B66	WAKE0#	C66	PEG_RX4-	D66	PEG_TX4-
A67	GPI2	B67	WAKE1#	C67	RSVD	D67	GND
A68	PCIE_TX0+	B68	PCIE_RX0+	C68	PEG_RX5+	D68	PEG_TX5+
A69	PCIE_TX0-	B69	PCIE_RX0-	C69	PEG_RX5-	D69	PEG_TX5-
A70	GND (FIXED)	B70	GND (FIXED)	C70	GND (FIXED)	D70	GND (FIXED)
A71	LVDS_A0+	B71	LVDS_B0+	C71	PEG_RX6+	D71	PEG_TX6+
A72	LVDS_A0-	B72	LVDS_B0-	C72	PEG_RX6-	D72	PEG_TX6-
A73	LVDS_A1+	B73	LVDS_B1+	C73	SDVO_DATA	D73	SDVO_CLK
A74	LVDS_A1-	B74	LVDS_B1-	C74	PEG_RX7+	D74	PEG_TX7+
A75	LVDS_A2+	B75	LVDS_B2+	C75	PEG_RX7-	D75	PEG_TX7-
A76	LVDS_A2-	B76	LVDS_B2-	C76	GND	D76	GND
A77	LVDS_VDD_EN	B77	LVDS_B3+	C77	RSVD	D77	IDE_CBLID#
A78	LVDS_A3+	B78	LVDS_B3-	C78	PEG_RX8+	D78	PEG_TX8+
A79	LVDS_A3-	B79	LVDS_BKLT_EN	C79	PEG_RX8-	D79	PEG_TX8-
A80	GND (FIXED)	B80	GND (FIXED)	C80	GND (FIXED)	D80	GND (FIXED)
A81	LVDS_A_CK+	B81	LVDS_B_CK+	C81	PEG_RX9+	D81	PEG_TX9+
A82	LVDS_A_CK-	B82	LVDS_B_CK-	C82	PEG_RX9-	D82	PEG_TX9-
A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL	C83	RSVD	D83	RSVD
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY	C84	GND	D84	GND
A85	GPI3	B85	VCC_5V_SBY	C85	PEG_RX10+	D85	PEG_TX10+
A86	KBD_RST#	B86	VCC_5V_SBY	C86	PEG_RX10-	D86	PEG_TX10-
A87	KBD_A20GATE	B87	VCC_5V_SBY	C87	GND	D87	GND
A88	PCIE0_CK_REF+	B88	BIOS_DIS1#	C88	PEG_RX11+	D88	PEG_TX11+
A89	PCIE0_CK_REF-	B89	VGA_RED	C89	PEG_RX11-	D89	PEG_TX11-
A90	GND (FIXED)	B90	GND (FIXED)	C90	GND (FIXED)	D90	GND (FIXED)
A91	SPI_POWER	B91	VGA_GRN	C91	PEG_RX12+	D91	PEG_TX12+
A92	SPI_MISO	B92	VGA_BLU	C92	PEG_RX12-	D92	PEG_TX12-
A93	GPO0	B93	VGA_HSYNC	C93	GND	D93	GND
A94	SPI_CLK	B94	VGA_VSYNC	C94	PEG_RX13+	D94	PEG_TX13+
A95	SPI_MOSI	B95	VGA_I2C_CK	C95	PEG_RX13-	D95	PEG_TX13-
A96	GND	B96	VGA_I2C_DAT	C96	GND	D96	GND
A97	Type 10 VCC_12V	B97	SPI_CS#	C97	RSVD	D97	PEG_ENABLE#
A98	RSVD VCC_12V	B98	RSVD	C98	PEG_RX14+	D98	PEG_TX14+
A99	RSVD VCC_12V	B99	RSVD	C99	PEG_RX14-	D99	PEG_TX14-
A100	GND (FIXED)	B100	GND (FIXED)	C100	GND (FIXED)	D100	GND (FIXED)
A101	RSVD VCC_12V	B101	RSVD VCC_12V	C101	PEG_RX15+	D101	PEG_TX15+
A102	RSVD VCC_12V	B102	RSVD VCC_12V	C102	PEG_RX15-	D102	PEG_TX15-
A103	RSVD VCC_12V	B103	RSVD VCC_12V	C103	GND	D103	GND
A104	VCC_12V	B104	VCC_12V	C104	VCC_12V	D104	VCC_12V
A105	VCC_12V	B105	VCC_12V	C105	VCC_12V	D105	VCC_12V
A106	VCC_12V	B106	VCC_12V	C106	VCC_12V	D106	VCC_12V
A107	VCC_12V	B107	VCC_12V	C107	VCC_12V	D107	VCC_12V
A108	VCC_12V	B108	VCC_12V	C108	VCC_12V	D108	VCC_12V
A109	VCC_12V	B109	VCC_12V	C109	VCC_12V	D109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)	C110	GND (FIXED)	D110	GND (FIXED)

	= not supported on MSC CXC-PV525 module

3 System resources

3.1 PCI IRQ Routing

4

			Interrupts of Controller (ICH-8M)							
Slot Number (or Onboard Device)	IDSEL # or DEV. #	Bus #	PIRQ 0 (INT A)	PIRQ 1 (INT B)	PIRQ 2 (INT C)	PIRQ 3 (INT D)	PIRQ 4 (INT E)	PIRQ 5 (INT F)	PIRQ 6 (INT G)	PIRQ 7 (INT H)
Internal Graphic	Dev 2 Fn 0	0	A							
GBit LAN Controller	Dev 19 Fn 0	0		A						
UHCI (USB1.1) Host										
USB Ports 0,1	Dev 29 Fn 0	0		A						
USB Ports 2,3	Dev 29 Fn 1	0			B					
USB Ports 4,5	Dev 29 Fn 2	0				C				
USB Ports 6,7	Dev 26 Fn 0	0			A					
EHCI (USB2.0) Host										
USB Ports 0-5	Dev 29 Fn 7	0		A						
USB Ports 6-7	Dev 26 Fn 7	0	C							
HD Audio	Dev 27 Fn 0	0				A				
PCIe x1 Root Port										
for Slot 1	Dev 28 Fn 0	0	A							
for Slot 2	Dev 28 Fn 1	0		B						
for Slot 3	Dev 28 Fn 2	0			C					
for Slot 4	Dev 28 Fn 3	0				D				
for Slot 5	Dev 28 Fn 4	0	A							
SATA Controller	Dev 31 Fn 2	0				B				
SMBus Controller	Dev 31 Fn 3	0	C							
PCIe x1 Slot 1	Dev 0 Fn 0	dyn	A	B	C	D				
PCIe x1 Slot 2	Dev 0 Fn 0	dyn	D	A	B	C				
PCIe x1 Slot 3	Dev 0 Fn 0	dyn	C	D	A	B				
PCIe x1 Slot 4	Dev 0 Fn 0	dyn	B	C	D	A				
PCIe x1 Slot 5	Dev 0 Fn 0	dyn	A	B	C	D				
PCI Slot 1	AD20 / Dev 4	dyn					A	B	C	D
PCI Slot 2	AD21 / Dev 5	dyn					D	A	B	C
PCI Slot 3	AD22 / Dev 6	dyn					C	D	A	B
PCI Slot 4	AD23 / Dev 7	dyn					B	C	D	A
PATA Controller	Dev 1F Fn 1	dyn			A					

3.2 Carrier Board PCI Resource Allocation

The external PCI resource allocation on the carrier board should be as follows:

Slot / Device Signal	Slot / Device 0	Slot / Device 1	Slot / Device 2	Slot / Device 3
IDSEL	PCI_AD[20]	PCI_AD[21]	PCI_AD[22]	PCI_AD[23]
PCI Clock	PCI_CLK replica	PCI_CLK replica	PCI_CLK replica	PCI_CLK replica
INTA#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#
INTB# (if used)	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#
INTC# (if used)	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#
INTD# (if used)	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#
REQ0# (if used)	PCI_REQ[0]#	PCI_REQ[1]#	PCI_REQ[2]#	PCI_REQ[3]#
REQ1# (if used)	PCI_REQ[1]#	PCI_REQ[2]#	PCI_REQ[3]#	PCI_REQ[0]#
REQ2# (if used)	PCI_REQ[2]#	PCI_REQ[3]#	PCI_REQ[0]#	PCI_REQ[1]#
REQ3# (if used)	PCI_REQ[3]#	PCI_REQ[0]#	PCI_REQ[1]#	PCI_REQ[2]#
GNT0# (if used)	PCI_GNT[0]#	PCI_GNT[1]#	PCI_GNT[2]#	PCI_GNT[3]#
GNT1# (if used)	PCI_GNT[1]#	PCI_GNT[2]#	PCI_GNT[3]#	PCI_GNT[0]#
GNT2# (if used)	PCI_GNT[2]#	PCI_GNT[3]#	PCI_GNT[0]#	PCI_GNT[1]#
GNT3# (if used)	PCI_GNT[3]#	PCI_GNT[0]#	PCI_GNT[1]#	PCI_GNT[2]#

The signals PCI_IRQx, PCI_REQx or PCI_GNTx are are routed exclusively to the COM Express connector. They are not shared on the CPU board.

3.3 SMB Address Map

Device	A6	A5	A4	A3	A2	A1	A0	R/W	address *)
SMBus host (ICH8-M slave)	0	0	0	1	0	0	0	x	10h / 08h
SMSC EMC2104	0	1	0	1	1	1	1	x	5Eh / 2Fh
Watchdog (PIC12C509)	1	0	1	1	0	0	0	x	B0h / 58h
ICS9LPRS365 Clock Synthesizer	1	1	0	1	0	0	1	x	D2h / 69h
CMOS backup EEPROM	1	0	1	0	1	0	0	x	A8h / 54h
SPD EEPROM (SO-DIMM)	1	0	1	0	0	0	0	x	A0h / 50h

*) 8 bit address (with R/W) / 7 bit address (without R/W)

4. Connectors

4.2 Connector X5 (FAN)

Pin	Signal
1	GND
2	PWM controlled VCC +12V
3	Fan speed

Connector: JST S3B-ZR-SM4A-TF

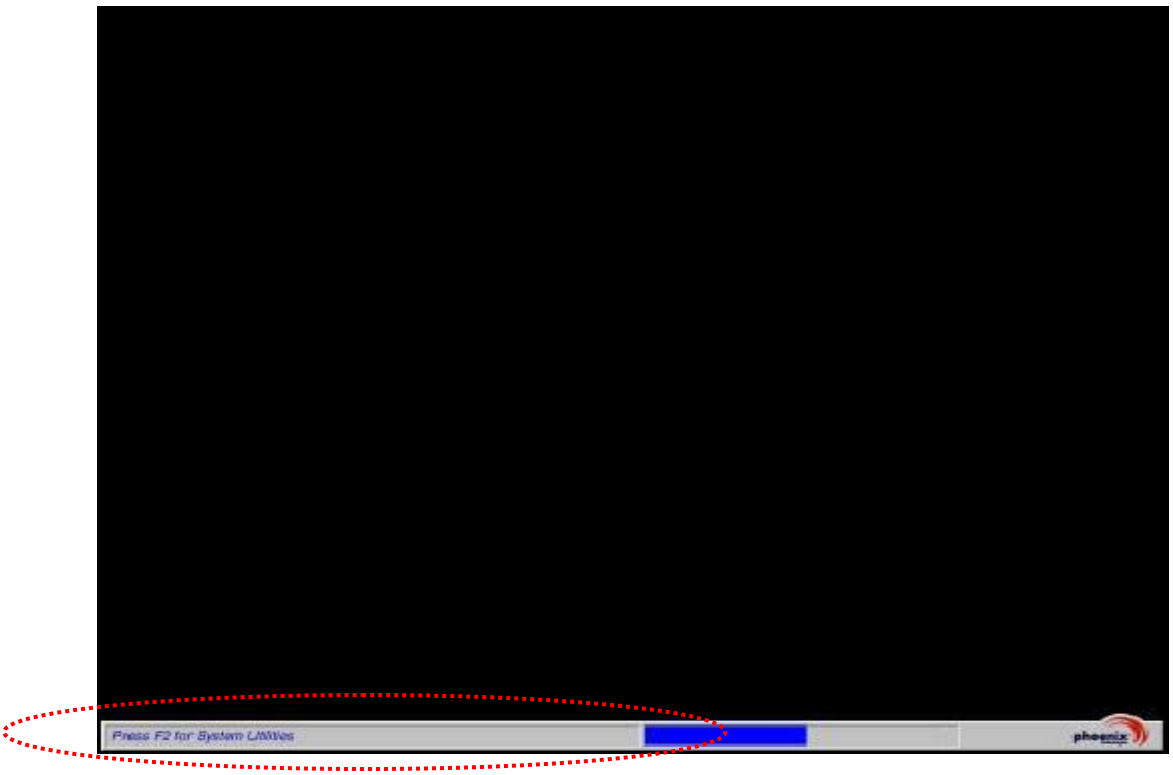
5. BIOS

5.2 Introduction

This guide describes the Phoenix TrustedCore Startup screen and contains information on how to access Phoenix TrustedCore setup to modify the settings which control Phoenix pre-OS (operating system) functions.

5.2.1 Startup Screen Overview

The Phoenix TrustedCore Startup screen is a graphical user interface (GUI) that is included in Phoenix TrustedCore products. The default bios behavior is to show an informational text screen during bios POST phase, but the graphical boot screen can be enabled in the bios setup. The standard boot screen is a black screen, including a progress bar at the bottom of the screen. This bar indicates the progress of the Startup Screen functions and provides user prompting and POST status. The following figure shows the various parts of a generic Startup Screen at 1024x768 resolution:



5.2.2 Activity Detection Background

While the TrustedCore Startup screen is displayed, press the Setup Entry key (F2 – TrustedCore default). The TrustedCore Startup Status Bar acknowledges the input, and at the end of POST, the screen clears and setup launches.
An example of the Startup Status Bar displaying changing state is shown in the following figure. The “Please Wait…” text is displayed after the F2 key is pressed to acknowledge user input.

Active status bar:

5.3 TrustedCore Setup Utility

With the Phoenix TrustedCore Setup program, you can modify TrustedCore settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning the special features on or off. This chapter provides an overview of the Setup utility and describes at a high-level how to use it.

5.3.1 Configuring the System BIOS

To start the Phoenix TrustedCore Setup utility, press [F2] to launch Setup. The Setup main menu appears.

The BIOS Menu Structure

The BIOS Menu is structured in the following way:

Main
Board Information
IDE Primary Master
IDE Primary Slave
SATA Port 1
SATA Port 2
SATA Port 3
Keyboard Features
Boot Features
Advanced
Cache Memory
CPU Control Sub-Menu
Video (Intel IGD) Control Sub-Menu
ICH Control Sub-Menu
PnP Configuration
ACPI Control Sub-Menu
Integrated Device Sub-Menu
PCI Express Control Sub-Menu
ICH USB Control Sub-Menu
I/O Device Configuration
Clock Control Sub-Menu
Watchdog Options
Security
Power
Hardware Monitor
Boot
Exit

The Menu Bar

The Menu Bar at the top of the window lists these options:

Menu Items	Description
Main	Use this menu for basic system configuration.
Advanced	Use this menu to set the Advanced Features available on the system's chipset.
Security	Use this menu to set User and Supervisor Passwords and configure optional TPM.
Power	Use this menu to configure Power-Management features.
Boot	Use this menu to set the boot order in which the BIOS attempts to boot to OS.
Exit	Exits the current menu.

Use the left and right arrow keys on your keyboard to make a menu selection.

The Legend Bar

Use the keys listed in the legend bar on the bottom of the screen to make your selections, or to exit the current menu. The following table describes the legend keys and their alternates:

Key	Function
F1 or Alt-H	General Help window.
Esc	Exit this menu.
Arrow keys left and right	Select a different menu.
Up and down arrow keys	Move cursor up and down.
Tab or Shift-Tab	Move cursor left and right (i.e. at System Time / System Date).
Home or End	Move cursor to top or bottom of window.
PgUp or PgDn	Move cursor to next or previous page.
F5 or -	Select the previous value for the field.
F6 or + or Space	Select the next value for the field.
F9	Load the Default Configuration values (for all menus).
F10	Save and exit.
Enter	Execute command or select Sub-Menu.

Select an item

To select an item, use the arrow keys to move the cursor to the field you want. Then use the plus-and-minus value keys to select a value for that field. The Save Values command in the Exit Menu saves the values currently displayed in all the menus.

Display a Sub-Menu

To display a Sub-Menu, use the arrow keys to move the cursor to the desired sub menu. Then press Enter.

Note: Bold and underlined setup options in this manual show the default value !

5.3.2 The Main Menu

The following selections can be made in the Main Menu.. Use the sub menus for further options.

Feature	Options	Description
Board Information	Sub-Menu	Displays BIOS Version
System Time	Enter Time (HH:MM:SS)	Set the System Time.
System Date	Enter Date (DD/MM/YYYY)	Set the System Date.
IDE Primary Master	Sub-Menu Drive Settings	Configure IDE Primary Master
IDE Primary Slave	Sub-Menu Drive Settings	Configure IDE Primary Slave
SATA Port 1	Sub-Menu Drive Settings	Configure SATA Port 1
SATA Port 2	Sub-Menu Drive Settings	Configure SATA Port 2
SATA Port 3	Sub-Menu Drive Settings	Configure SATA Port 3
Boot Features	Sub-Menu	Configure Boot Features
Keyboard Features	Sub-Menu	Configure Keyboard Features

5.3.2.1 Board Information

Feature	Options	Description
Bios Version	Informative	Shows current bios version.
HW Platform	Informative	Name of the hardware platform
HW Revision	Informative	Hardware revision number
Serial #	Informative	Hardware Serial Number
MAC Address	Informative	Shows MAC Address
Boot Counter	Informative	The number of times this board has booted up.
CPU String	Informative	CPU Identification string
CPU Speed	Informative	CPU Speed
CPU Family	Informative	CPU ID Family code
CPU Model	Informative	CPU ID Model code
CPU Stepping	Informative	CPU ID Stepping
CPU Cores	Informative	Number of CPU cores
Microcode Patch ID	Informative	CPU Microcode ID
Installed Memory	Informative	Shows installed Memory
Used by Devices	Informative	Shows Memory used by Devices
System Memory	Informative	Amount of memory below 1MB
Extended Memory	Informative	Total amount of memory
UUID	Informative	Shows UUID of module

5.3.2.2 Drive Settings

The drive settings on the Main Menu control the following device types:

- **Hard-disk drives (IDE and SATA)**
- **Removable-disk drives**
- **CD-ROM drives**

There is one IDE connector on the motherboard, usually labeled "Primary IDE". There are usually two connectors on each ribbon cable attached to IDE connector. When you have connected two drives to this connector, the one on the end of the cable is the Master.

When entering Setup, the Main Menu displays the results of **Autotyping** information each drive provides its own size and other characteristics–and whether it is configured as a Master or Slave on the system.

Note: Do not attempt to change these settings unless you have an installed drive that does not autotype properly (such as an older hard-disk drive that does not support autotyping).

If you need to change the drive settings, select one of the Master or Slave drives on the Main Menu. This will display a menu like this:

Note: The capacity is displayed in 'real' Mbytes (1MB=1024*1024 Bytes) Drives with a total capacity greater than 8Gbyte operate in LBA format only.

Feature	Options	Description
Type	None, ATAPI Removable, CD-ROM, IDE Removable, Other ATAPI, User, **Auto**	None = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed. Auto = Autotyping, the drive itself supplies the information. User = You supply the hard-disk drive information in the following fields. ATAPI Removable = Removable Disk Drive Other ATAPI = non-specific ATAPI Device CD-ROM = CD-ROM drive.
Cylinders	1 to 65536 (only informative)	Number of Cylinders
Heads	1 to 16 (only informative)	Number of read/write heads
Sectors	1 to 63 (only informative)	Number of sectors per track
Multi-Sector Transfers	Disabled, 2 sectors, 4 sectors, 8 sectors, 16 sectors	Any selection except Disabled determines the number of sectors transferred per block.

Feature	Options	Description
LBA Mode Control	Disabled, Enabled	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, & Sectors.
32 Bit I/O	**Disabled**, Enabled	Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus.
Transfer Mode	Standard Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO 3 / DMA 1 FPIO 4 / DMA 2	Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.
Ultra DMA Mode	Disabled Mode 0 Mode 1 Mode 2 Mode 3 Mode 4 Mode 5	Ultra DMA Mode supports 33/66/100 MB/sec transfer rate for fixed disk drives.
SMART Monitoring	Disabled, Enabled	Displays the status of SMART Monitoring if supported by the used drive.

WARNING: Incorrect settings can cause your system to malfunction.

5.3.2.3 Keyboard Features

Feature	Options	Description
NumLock	**Auto**, On, Off	Selects Power-on state for NumLock
Key Click	**Disabled**, Enabled	Enables or disables key click feature
Keyboard auto-repeat rate	**30/sec**, 26.7/sec, 21.8/sec, 18.5/sec, 13.3/sec, 10/sec, 6/sec, 2/sec	Selects key repeat rate
Keyboard auto-repeat delay	¼ sec, **½ sec**, ¾ sec, 1 sec	Selects delay before key repeat

5.3.2.4 Boot Features

Feature	Options	Description
Summary screen	**Disabled**, Enabled	Enabled displays system configuration on boot.
Boot-time Diagnostic Screen	Disabled, **Enabled**	Enabled displays the diagnostic screen during boot. Disabled displays the Boot Logo.
Quick Boot Mode	Disabled, **Enabled**	Allows the System to skip certain tests while booting. This will decrease the time needed to boot the system.
Post Errors	Disabled, **Enabled**	Pauses and displays Setup Entry or resume boot prompt if error occurs on boot. If disabled, system always attempts to boot.
Extended Memory Testing	Normal, Just zero it, **None**	Determines which type of test will be performed on extended memory during POST (above 1 MB).

5.3.3 The Advanced Menu

Feature	Options	Description
Installed O/S	**Other,** Win95, Win98, WinMe, Win2000, WinXP	Select the operating system installed on your system which you will use most commonly. **NOTE**: An incorrect setting can cause some operating systems to display unexpected behavior.
Reset configuration Data	**No**, Yes	Select 'Yes' if you want to clear the Extended System Configuration Data (ESCD) area.
Large Disk Access Mode	Other, **DOS**	Select Other for UNIX, Novell NetWare. Select DOS for all other operating systems.

Feature	Options	Description
Small LBA-Disk Access Mode	**No**, Yes	Select if CHS translation should be made for a LBA-capable harddisk with less than 1024 cylinders, e.g. CompactFlash(R). If you have problems with booting from a CompactFlash(R), try to change this setting. No = translate CHS only if HDD has >1024 cyls. Yes = translate CHS for all LBA-capable disks.
Legacy USB Support	**Enabled**, Disbaled	Enable support for Legacy Universal Serial Bus
Cache Memory	Sub-Menu	Configures Cache Memory
CPU Control Sub-Menu	Sub-Menu	Configure CPU Control
Video (Intel IGD) Control Sub-Menu	Sub-Menu	Configure Video (Intel IGD) Control
ICH Control Sub-Menu	Sub-Menu	Configure ICH Control
ACPI Control Sub-Menu	Sub-Menu	Configure ACPI Control
Integrated Device Control Sub-Menu	Sub-Menu	Configure Integrated Device Control
I/O Device Configuration	Sub-Menu	Configure I/O Device
Clock Control Sub-Menu	Sub-Menu	Configure Clock Control
Watchdog Options	Sub-Menu	Configure Watchdog Options

5.3.3.1 Cache Memory

Feature	Options	Description
Cache System Bios area	Uncached, **Write Protect**	Controls caching of system bios area
Cache Video Bios area	Uncached, **Write Protect**	Controls caching of video bios area
Cache D000 – D3FF Cache D400 – D7FF Cache D800 – DBFF Cache DC00 - DFFF	**Disabled**, Write Through, Write Protect, Write Back	Disabled = This block is not cached. Write through = Writes are cached and sent to main memory at once. Write Protect = Writes are ignored. Write Back = Writes are cached but not sent to main memory until necessary.

5.3.3.2 CPU Control Sub-Menu

Note: Some options can be different dependent on used type of CPU !

Feature	Options	Description
Hyperthreading	Disabled, **Enabled**	Enabling Hyperthreading activates additional CPU threads. These threads may appear as additional processors but will share some resources with other threads within the physical package.
Processor Power Management	Disabled, GV3 only, C-States Only, **Enabled**	Selects the Processor Power Management desired: Disabled = C-States and GV3 are disabled. GV3 Only = C-States are disabled. C-States Only = GV3 is disabled. Enabled = C-States und GV3 are enabled. Note: GV3 refers to the speed step capability of the CPU. Only N455 supports GV3. Note: For optimal response times Power Management must be disabled.
Enhanced C-States Enable	**Enabled**, Disabled	Enables Enhanced C-State

Feature	Options	Description
C-State Residency	Enabled, **Disabled**	Enables C-State Residency for Intel tool.
No Execute Mode Mem Protection	**Enabled**, Disabled	When enabled and OS supports the feature, the OS can set memory pages as not executable.
Set Max Ext CPUID = 3	**Disabled**, Enabled	Sets Max CPUID extended function value to 3.

5.3.3.3 Video (Intel IGD) Control Sub-Menu

Feature	Options	Description
Default Primary Video Adapter	**Auto**, IGD	Select Auto to have Internal Graphics if supported and enabled, be used for the boot display device. If PCI Video Card is connected, PCI Video will be used. Select IGD to use internal graphics if PCI Video Card is connected.
IGD – Device 2	Disabled, **Auto**	Enables or Disable the Internal Graphics Device by setting item to the desired value.
IGD – Device 2, Function1	Disabled, **Auto**	Enables or Disable Function 1 of the Internal Graphics Device by setting item to the desired value.
IGD – Boot Type	**VBT default**, CRT, LFP , CRT+LFP	Select the Video Device that will be activated during POST.
IGD – LCD Panel Type	640x480, sp, 18bit 800x600, sp, 18bit **1024x768 sp, 18bit** 800x480, sp,18bit 1280x800, sp,18bit 1366x768, sp,18bit	Select the Local Flat Panel used by the Internal Graphics Device by selecting the appropriate setup item. First Item is Panel 1, the last item is panel 6.
IGD – Panel Scaling	**Auto**, Force Scaling, Off	Selects the LCD panel scaling option used by the Internal Graphics Device. 1. Auto 2. Force Scaling 3. Off

Feature	Options	Description
IGD Backlight Brightness	0%, 10%, … **100%**	Select the initial brightness for the LVDS backlight signal.
DVMT 4.0 Mode	Fixed, DVMT, **Auto**	Select the configuration of DVMT 4.0 Graphics Memory that Driver will allocate for use by the Internal Graphics Device. 1. Fixed 2. DVMT 3. Auto
Pre-Allocated Memory Size	**8 MB**	Select the amount of Pre-Allocated Graphics Memory for use by the Internal Graphics Device.
IGD Memory Size	**128 MB**, 256 MB MaxDVMT (only if DVMT Mode is selected)	Select the amount of Total Graphics Memory Pre-Allocated + Fixed + DVMT for use by the Internal for use by the Internal Graphics Device.
DVMT Graphics Memory	N/A	Displays the Memory size of the Video device.
Onboard EDID EEPROM	**Disabled**, Enabled	Enables or disables the Onboard EDID EEPROM for LFP.

5.3.3.4 ICH Control Sub Menu

Feature	Options	Description
PnP Configuration	Sub-Menu	Configure PCI Control
DMI Link ASPM Control	**Disabled**, Enabled	Enable/Disable the Active State Power Management on DMI Link between CPU and ICH8M. If Enabled it may slightly reduce power consumption, but may slightly delay PCI or PCIe access cycles.
Pop Up Mode Enable	**Disabled**, Enabled	Select the proper mode: If disabled, bus master traffic is a break event and it will return from C3/C4 to C0 based on break events. If enabled, ICH will observe a bus master request and it will take the system from a C3/C4 state to a C2 state and auto enable bus masters.

Feature	Options	Description
Pop Down Mode Enable	Disabled, **Enabled**	Should be enabled only if Pop up is enabled: If disabled, ICH will NOT attempt to automatically return. If enabled, ICH will observe a NO bus master request and it can return to a previous C3 or C4 state.
Port 80h Cycles	**LPC BUS**, PCI BUS	Control where Port 80h cycles are sent

5.3.3.5 PNP Configuration

Feature	Options	Description
PCI IRQ line 0:	**Auto Select**, 3, 4, 5, 6, 7, 10, 11 ,12	Select which interrupt should be assigned to this PCI IRQ. Devices: IGD, EHCI Controller 2, SMBus, PCIe Port 1, PCIe Port5
PCI IRQ line 1:	**Auto Select**, 3, 4, 5, 6, 7, 10, 11 ,12	Select which interrupt should be assigned to this PCI IRQ. Devices: Onboard Lan, UHCI Controller1, EHCI Controller 1, PCIe Port 2,
PCI IRQ line 2:	**Auto Select**, 3, 4, 5, 6, 7, 10, 11 ,12	Select which interrupt should be assigned to this PCI IRQ. Devices: ICH PATA Controller, UHCI Controller 2, UHCI Controller 4, PCIe Port 3
PCI IRQ line 3:	**Auto Select**, 3, 4, 5, 6, 7, 10, 11 ,12	Select which interrupt should be assigned to this PCI IRQ. Devices: ICH SATA Controller, HD Audio, UHCI Controller 3, PCIe Port 4
PCI IRQ line 4:	**Auto Select**, 3, 4, 5, 6, 7, 10, 11 ,12	Select which interrupt should be assigned to this PCI IRQ. Devices: PCI Slot 1
PCI IRQ line 5:	**Auto Select**, 3, 4, 5, 6, 7, 10, 11 ,12	Select which interrupt should be assigned to this PCI IRQ. Devices: PCI Slot 2
PCI IRQ line 6:	**Auto Select**, 3, 4, 5, 6, 7, 10, 11 ,12	Select which interrupt should be assigned to this PCI IRQ. Devices: : PCI Slot 3
PCI IRQ line 7:	**Auto Select**, 3, 4, 5, 6, 7, 10, 11 ,12	Select which interrupt should be assigned to this PCI IRQ. Devices: : PCI Slot 4

5.3.3.6 ACPI Control Sub-Menu

Feature	Options	Description
Disable ACPI _Sx	**None**, S1, S2, S3, S5	Select one of the ACPI power states: S1, S2,S3, S5. If selected, the corresponding power state will be disabled.
FACP – RTC S4 Flag Value	Disabled, **Enabled**	Valid only for ACPI Control the value for the RTC S4 flag in the FACP Table
FACP – PM Timer Flag Value	Disabled, **Enabled**	Valid only for ACPI Controls the timer used by the OS through the FACP Tables Flags. This is now possible with WINXP SP2 and beyond.
HPET Support	Disabled, **Enabled**	This field is valid only in the WindowsXP OS. Control the High Performance Event Timer through this setup option when enabled. The HPET Table will then be pointed to by the RSDT and the proper enable bits will be set.
HPET Base Address	**0xFED00000**, 0xFED01000, 0xFED02000, 0xFED03000	Select the Base Address for the High Performance Event Timer.

5.3.3.7 Integrated Device Control Sub-Menu

Feature	Options	Description
PCI Express Control Sub-Menu	Sub-Menu	Configure PCIe Control
ICH USB Control Sub-Menu	Sub-Menu	Configure USB Control
Azalia Audio	Disabled, **Auto**	Enables or disables onboard HD Audio
Parallel ATA	**Enabled**, Disabled	Enables or Disables onboard PATA Controller
SATA Solid State Disk:	Disabled Read / Only **Read / Write**	Local Solid State Disk (SSD) on SATA Port 3 Set to 'Disabled' to Power down SSD device.
SATA Raid	**Disabled**, Enabled	Enables SATA Raid Oprom. To enter Raid Option Rom Setup press CTRL-J after Post. After your Raid-Set (0,1) is built exit the Raid Option Rom. The Raid Volume will appear as PCI SCSI device in the Boot Menu. For XP installation a floppy is required to load AHCI driver during setup by pressing F6. Vista und Win7 have built in drivers for installation. It is recommended to install Intel Matrix Storage Utility after installation of Windows.
SATA AHCI Configuration	**Disabled**, Enabled	Enables AHCI. For XP installation a floppy is required to load AHCI driver during setup by pressing F6. Vista und Win7 have built in drivers for installation.
Disable Vacant Ports	**Disabled**, Enabled	Controls automatic disabling if vacant SATA ports.
On–board LAN	Disabled, **Enabled**	Controls Power to the onboard device. Note: Re-enabling the LAN after it has been disabled requires platform power cyvling.

Feature	Options	Description
PXE OPROM	**Disabled**, Enabled	Enable PXE Option ROM.

5.3.3.7.1 PCI Express Sub-Menu

Feature	Options	Description
PCI Express – Root Port 1	**Auto**, Enabled, Disabled	Control the PCI Express Port via this setup option. Disabled – Port always disabled Auto – Only enabled if card found Note that if Root Port 1 is disabled, Root Ports 2-5 will be disabled as well.
PCI Express – Root Port 2	**Auto**, Enabled, Disabled	Control the PCI Express Port via this setup option. Disabled – Port always disabled Auto – Only enabled if card found
PCI Express – Root Port 3	**Auto**, Enabled, Disabled	Control the PCI Express Port via this setup option. Disabled – Port always disabled Auto – Only enabled if card found
PCI Express – Root Port 4	**Auto**, Enabled, Disabled	Control the PCI Express Port via this setup option. Disabled – Port always disabled Auto – Only enabled if card found
PCI Express – Root Port 5	**Auto**, Enabled, Disabled	Control the PCI Express Port via this setup option. Disabled – Port always disabled Auto – Only enabled if card found
Root Port ASPM Support	Auto, **Disabled**	Control ASPM support for all the enabled Root Ports. Auto = will set APMC to the highest common supported ASPM between the Port and Endpoint.

5.3.3.7.2 ICH USB Control Sub-Menu

Feature	Options	Description
USB Ports 0-5	Ports 0-1, Ports 0-3, **Ports 0-5**	Select USB Ports that should be available by USB controller Device 29
USB 2.0 Ports 0-5	**Enabled**, Disabled	Enables USB 2.0 (EHCI) functionality on ports 0-5
USB 2.0 Ports 6-7	**Enabled 6-7**, Disabled	Select USB Ports that should be available by USB controller Device 26.

5.3.3.8 I/O Device Configuration Menu

Feature	Options	Description
Serial Port A	**Disabled**, Enabled,	Disabled = Disables the device Enabled = User configuration
Base I/O address	**3F8**, 2F8, 3E8, 2E8	Set the base I/O address for Serial Port A.
Interrupt	3, **4**	Set the interrupt for Serial Port A.
Serial Port B	**Disabled**, Enabled	Disabled = Disables the device Enabled = User configuration
Mode	**Normal**, IR, ASK-IR	Set the mode for Serial Port B (wired / infrared).
Base I/O address	3F8, **2F8**, 3E8, 2E8	Set the base I/O address for Serial Port B.
Interrupt	**3**, 4	Set the interrupt for Serial Port B.
Parallel Port	**Disabled**, Enabled, Auto	Configure parallel port using options: Disabled = No configuration Enabled = User configuration
Mode	**Output only**, Bi-directional, ECP	Set the mode for the parallel port using options: Output only, Bi-directional, ECP
Base I/O address	**378**, 278, 3BC	Set the base I/O address for the parallel port.

Feature	Options	Description
Interrupt	5, **7**	Set the interrupt for the parallel port.
DMA channel	**DMA 3**, DMA 1	Set the DMA channel for the parallel port.
PS/2 Mouse Emulation	**Disabled**, Enabled	'Disabled' disables PS/2 mouse emulation and frees up IRQ 12 'Enabled' allows mouse driver functionality for DOS by emulating PS/2 mouse using IRQ 12.

Warning: If the same I/O address or Interrupt is selected for more than one port, the menu displays an asterisk (*) for the conflicting settings.

5.3.3.9 Clock Control Sub-Menu

Feature	Options	Description
CK-505 Clock Chip	Default, **Program**	Control Programming of the CK-505 Clock Chip. Program = program values by Bios Default= Use default values at Power-On
Spread Spectrum mode	**Off**, On	Control programming of the Spread Spectrum Mode bit in CK-505 chip. 0.5% Downspread if enabled.

5.3.3.10 Watchdog Options

Feature	Options	Description
Watchdog delay	1 second, 5 seconds, 10 seconds, **30 seconds** 1 minute , 5 minutes, 10 minutes, 30 minutes	After the watchdog is activated, it waits the selected delay time before it starts decrementing the timeout period.

Feature	Options	Description
Watchdog timeout	0.4 second, 1 second, 5 seconds, 10 seconds, **30 seconds**, 1 minute , 5 minutes, 10 minutes	Select the maximum watchdog trigger period. If the watchdog is not triggered before the end of this period, a system reset will be generated.
Watchdog start on boot	**No**, Yes	Select if the watchdog should be started at the end of POST.

5.3.4 The Security Menu

Feature	Options	Description
Supervisor Password Is:	Displays Supervisor Password	Displays the current status of the Supervisor password (“Clear” or “Set”)
User Password Is:	Displays User Password	Displays the current status of the User password (“Clear” or “Set”)
Set Supervisor Password	Press return to enter supervisor password	Supervisor Password controls access to the setup utility.
Set User Password	Press return to enter user password	User Password controls access to the system at boot.
Password on boot	**Disabled**, Enabled	Enables password entry on boot
TPM Support	**Disabled**, Enabled	Enable Trusted Platform Module support. **Note:** TPM options will only be available if TPM is assembled.
Current TPM State	Displays Current TPM State	Displays the current TPM status.
Change TPM State	**No Change**, Enable & Activate, Deactivate & Disable, Clear	Changes TPM state.

5.3.5 The Power Menu

Feature	Options	Description
After Power Failure	Stay Off, **Power On**	Sets the mode of operation if an AC power loss occurs. Power On will turn the power on as soon as the power supply is back on. Stay Off will keep the power off until the power button is pressed.
Hardware Monitor	Sub-Menu	Configure Hardware Monitor

5.3.5.1 Hardware Monitor

Feature	Description
Supply Voltage (+12V)	Displays the current CPU voltage.
CPU Core Temperature Sensor	Displays the current CPU temperature.
Memory Temperature Sensor	Displays the current Memory Temperature.
Board Temperature Sensor	Displays the current board temperature.
FAN Speed	Displays the current fan speed.

Feature	Options	Description
Fan Control	Disabled, **Auto**	Fan Cruise Control Auto: Fan speed is automatically controlled by temperature Disabled: Fan set to maximum speed
Fan Speed Zone 2	**20%**, 30%, 40% Fan Speed	Fan speed control for temperature zone 2. Temperature Zone 2 = 40°C – 50°C
Fan Speed Zone 3	**50%**, 60%, 70% Fan Speed	Fan speed control for temperature zone 3 (Medium temperature) Temperature Zone 3 = 50°C – 60°C **Note**: At Temperature Zone 4 (= >60°C) Fan speed is 100%

5.3.6 The Boot Menu

After you turn on the computer, it will attempt to load the operating system (eg. DOS, Windows XP, Linux, …) from a device listed in the boot priority order. If it cannot find the operating system on that device, it will attempt to load from the next device in the list.
Boot devices (i.e., with access to an operating system) can include: hard drives, floppy drives, CD ROMs, removable devices (e.g. USB sticks), and network cards.

Note: Specifying a device as a boot device on the Boot Menu requires that an operating system is loaded on that device.

Selecting "Boot" from the Menu Bar displays the Boot menu, which looks like this:

Feature	Description
Boot priority order: 1: USB KEY: 2: USB HDD: 3: USB CDROM: 4: IDE HDD: 5: IDE CD: 6: PCI SCSI: 7: PCI BEV: Note: This is the default boot order you see	Boot priority order for next boot. System tries to boot the first bootable device in this list. Use <+> and <-> to change order. Use <x> to exclude or include a device from/to the boot priority list. Use <Shift + 1> to enable or disable a device. Use <1 – 4> to load default boot sequence.
Exclude from boot order: : USB FDC : USB LS120 : Legacy Network Card : Bootable Add-in Cards	System does not try to boot a device from this list.

Pressing the “F10” key during the bios boot phase will bring up the bios boot menu, which will allow you to select a different boot device for the current boot process only. In this boot menu, only devices in the “Boot priority list” will be selectable. Devices excluded from the boot order will not be shown.

5.3.7 The Exit Menu

The following sections describe each of the options on this menu. Note that <Esc> does not exit this menu. You must select one of the items from the menu or menu bar to exit.

Exit Saving Changes

After making the selections in the Setup menus, always select "Exit Saving Changes". This procedure stores the options displayed in the menus in CMOS (battery-backed CMOS RAM) a special section of memory that stays alive after you turn the system off. The next time you boot the computer, the BIOS configures the system according to the Setup parameters stored in CMOS.
If you attempt to exit without saving, the program asks if you want to save before exiting. During boot-up, the Phoenix BIOS attempts to load the values saved in CMOS. If those values cause the system boot to fail, reboot and press <F2> to enter Setup. In Setup, you can reload the Default Values (as described below) or try to change the selections that caused the boot to fail.

Exit Discarding Changes

Use this option to exit Setup without storing in CMOS any new selections have been made. The selections previously in effect remain valid.

Load Setup Defaults

To display the default values for all the Setup menus, select "Load Setup Defaults" from the Main Menu.
If, during boot-up, the BIOS program detects a problem in the integrity of values stored in CMOS, it displays this message:

System CMOS checksum bad - run SETUP Press <F1> to resume, <F2> to Setup

The CMOS values have been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS.
Press <F1> to continue the boot process with the ROM default values already loaded or <F2> to run Setup and change the current settings.

Discard Changes

If, during a Setup Session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values previously saved to CMOS.
Selecting “Discard Changes” on the Exit menu restores all the selections to their previous values.

Save Changes

Selecting “Save Changes” saves all the selections without exiting Setup. You can return to the other menus if you want to review and change the selections.

5.4 Bios Update

If a System-BIOS update is required please follow these instructions:

1.) Create a bootable DOS disk/usb-stick/hdd.
Tested with DOS6.22 and DOS7.1. Do not use DOSKEY and XMS memory manager.

2.) Copy PHLASH16.EXE, BIOS.WPH and UPDATE.BAT to this device.

3.) Boot the system from this device.

4.) Type "update.bat" to update the System BIOS.

Note : If a window with UUID message pops up, press enter to skip this message. Otherwise it takes up to one minute till this message window closes automatically. When the UUID message window is closed, the bios update process continues.

5.) When the BIOS update has finished, reboot the system.

Note: After the system has been updated, the CMOS settings are changed back to default values and therefore it is necessary to enter Setup (press F2 at boot time) to reconfigure the system settings.

5.5 Bios Crisis Recovery

Should the BIOS setup be altered, such that it is no longer possible to re-enter the BIOS setup – for example if the wrong display is selected, the following methods can be used to restore the default settings:

1. Blind reset to defaults
2. Crisis recovery / clear backup EEPROM jumper
3. Crisis recovery software (usually only necessary if the BIOS is corrupted – for example if power was removed during a BIOS update)

5.5.1 Blind Reset to defaults

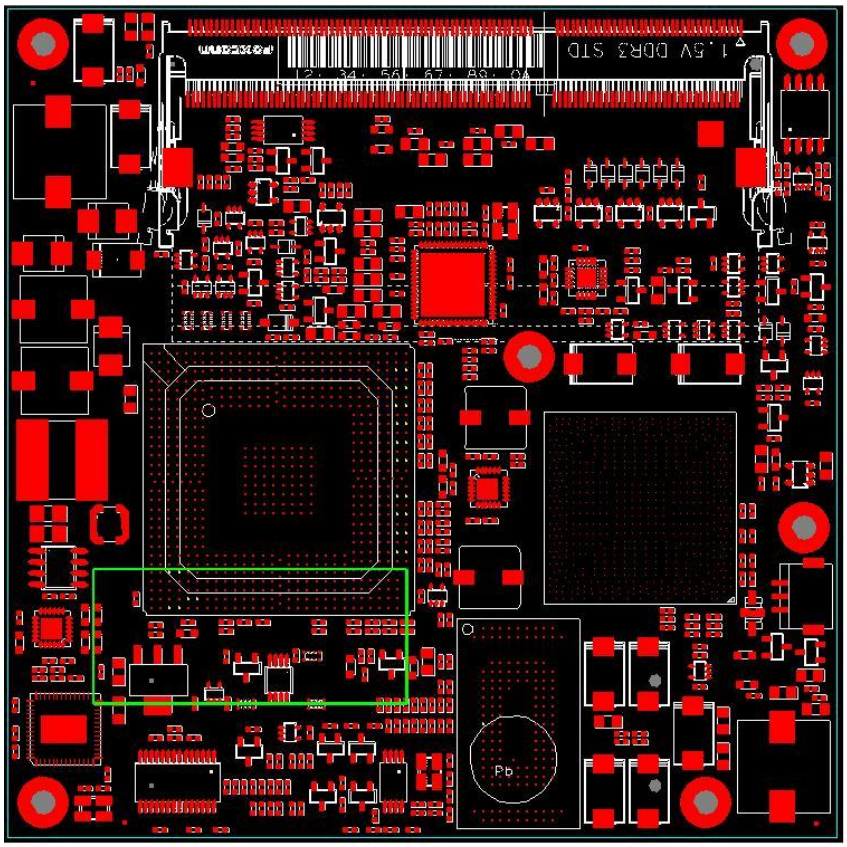
In the event that there is no display or the display is for some reason not active, in order to get the BIOS back to the default settings (and so enable the display) the following sequence must be performed:

1. During boot, press F2 to get into BIOS setup (F2 can be pressed repeatedly, if a beeper is installed, press F2 until setup entry will be signalled with a beep)
2. Press F9 and then enter to reset to default settings
3. Press F10 and then enter to save and exit the BIOS setup
4. System should then reboot with the default settings.

5.5.2 Crisis Recovery / Clear backup EEPROM Jumper

See photo below to find the Crisis Recovery or Clear backup EEPROM Jumper.
The two pads of this jumper should be shorted (using tweezers or pliers) before applying power to the board and held shorted until the crisis recovery has started. As soon as crisis recovery is started (indicated by a long beep) the short can be removed and the system can be restarted.

It is also possible to use a recovery USB dongle instead of shorting the jumper to reset the EEPROM. An USB dongle can be obtained from MSC.



5.5.3 Crisis Recovery software

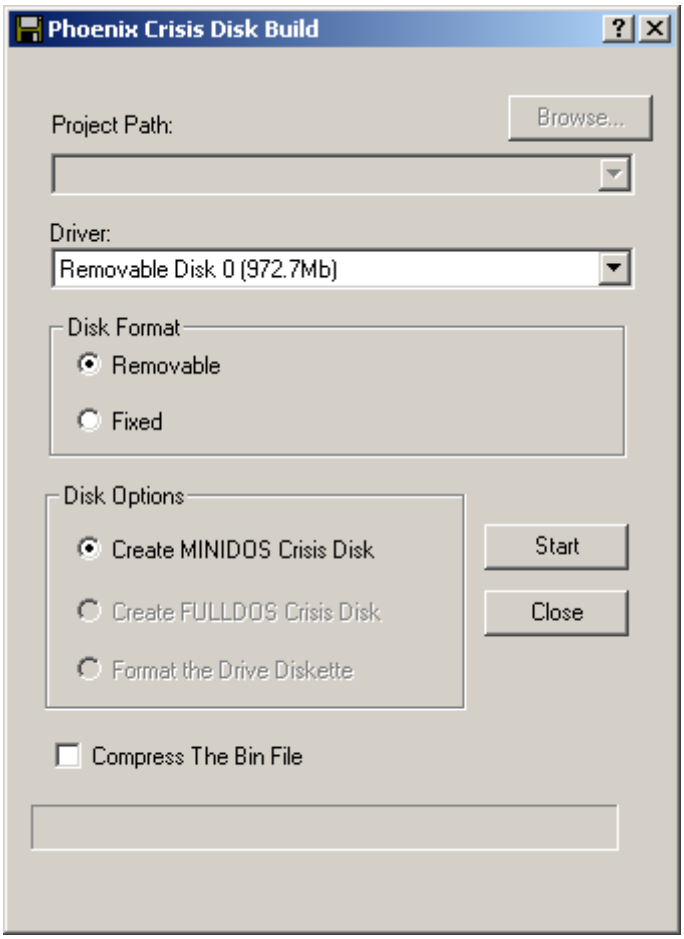
This technique should only be required in the event of a serious corruption of the BIOS – for example following an unsuccessful attempt to update the BIOS

To use this technique a special software – CRISDISK and a USB dongle must be obtained from MSC.

Note: Contact the MSC customer support for information how to obtain the CRISDISK.ZIP software and the USB recovery dongle.

Please follow these simple steps to create a bootable crisis recovery medium:

1. Unzip CRISDISK.ZIP and start the windows-based program WINCRIS.EXE on the host system. A window will pop up as shown below:



2. In the drop-down box, select “Removable Disk 0 (xxxMb)” to create a recovery USB stick. Disk options should be left as “Create MINIDOS Crisis Disk”.

3. Press the start button to generate the selected crisis recovery medium.

Proceed as follows to use the generated USB stick for the recovery :

Plug the USB dongle into a free USB port on the failing system before switching the system on. Please make sure that you use different USB controllers for USB dongle and USB crisis recovery medium. After power-up, crisis recovery mode should start automatically.

The programming process is signalled by short beeps and terminated after successfull programming with one long beep. To avoid a recovery loop it is recommended to remove the USB Controller after the first long beep after programming has been started.
After the second long beep, the system is automatically rebooted.

Important Notes:

USB recovery dongle and USB crisis recovery device must not be plugged into the same USB controller.

Crisis recovery may take up to 5 minutes

A long beep indicates a successful recovery.

Crisis recovery does not include the bootblock.

5.6 Diagnostics Postcodes

Postcodes can be seen on a special Postcode display, either on the MSC mainboard or on an external Postcode PCI card. There is an item in the bios setup to select the bus that should receive the postcode data: either PCI (for external cards) or LPC (for onboard displays).

If a postcode display has only 2 digits, only the lower byte of word-value postcodes will be shown.

5.6.1 Bootblock Bios Postcodes

Code	Bootblock Task Description
BBH	Bootblock Early Init after Reset
80h	Chipset Init
81h	Bridge Init
82h	CPU Init
83h	System Timer Init
84h	System I/O Init
85h	Check forced Recovery Boot, CMOS & CMOS Backup Clear
86h	Check BIOS Checksum
87h	Goto BIOS, start early BIOS initialzations
88h	Init Multi Processor
89h	Set Huge Segment
8Ah	OEM Initializations
8Bh	Init Interrupt and DMA Controller
8Ch	Init Memory Type
8Dh	Init Memory Size
8Eh	Shadow Boot Block
8Fh	Init SMM
90h	System Memory Test
91h	Init Interrupt Vectors
92h	Init Realtime Clock
93h	Init Standard Video
94h	Init Beeper
95h	Initialize USB Controller
95h	Init Boot
96h	Clear Huge Segment
97h	Boot OS
99h	Init Security

5.6.2 System Bios Postcodes

Code	Beeps	POST Task Description
04h		Get CPU type
03h		Disable Non-Maskable Interrupt (NMI)
06h		Initialize system hardware
07h		Disable shadow and execute code from the ROM.
08h		Initialize chipset with initial POST values
09h		Set IN POST flag
0Ah		Initialize CPU registers
0Bh		Enable CPU cache
0Ch		Initialize caches to initial POST values
0Eh		Initialize I/O component

Code	Beeps	POST Task Description
0Fh		Initialize fixed disk drives
10h		Initialize Power Management
11h		Load alternate registers with initial POST values
12h		Restore CPU control word during warm boot
13h		Initialize PCI Bus Mastering devices
14h		Initialize keyboard controller
16h	1-2-2-3	BIOS ROM checksum
17h		Initialize cache before memory Autosize
18h		8254 timer initialization
1Ah		8237 DMA controller initialization
1Ch		Reset Programmable Interrupt Controller
20h	1-3-1-1	Test DRAM refresh
22h	1-3-1-3	Test 8742 Keyboard Controller
24h		Set ES segment register to 4 GB
28h		Autosize DRAM
29h		Initialize POST Memory Manager
2Ah		Clear 512 kB Base RAM
2Ch	1-3-4-1	RAM Address test
2Eh	1-3-4-3	Base RAM Test
2Fh		Enable cache before system BIOS shadow
32h		Compute CPU clock speed in MHz
33h		Initialize Phoenix Dispatch Manager
36h		Warm start shut down
38h		Shadow system BIOS ROM
3Ah		Autosize cache
3Ch		Advanced configuration of chipset registers
3Dh		Load alternate registers with CMOS values
41h		Initialize RomPilot
42h		Initialize interrupt vectors
45h		POST device initialization
46h	2-1-2-3	Check ROM copyright notice
47h		Initialize I20 support
48h		Check video configuration against CMOS
49h		Initialize PCI bus and devices
4Ah		Initialize all video adapters in system
4Bh		QuietBoot start (optional)
4Ch		Shadow video BIOS ROM
4Eh		Display BIOS copyright notice
4Fh		Initialize MultiBoot
50h		Display CPU type and speed
51h		Initialize EISA board
52h		Test keyboard
54h		Set key click if enabled
55h		Configure USB devices
58h	2-2-3-1	Test for unexpected interrupts
59h		Initialize POST display service
5Ah		Display prompt "Press F2 to enter SETUP"
5Bh		Disable CPU cache
5Ch		Conventional memory test
60h		Extended memory test
62h		Address Test on Extended Memory
64h		Jump to UserPatch1
66h		Configure advanced cache registers
67h		CPU feature, MP, and APIC initialization
68h		Enable external and CPU caches

Code	Beeps	POST Task Description
69h		Setup System Management Mode (SMM) area
6Ah		Display external L2 cache size
6Bh		Load custom defaults (optional)
6Ch		Display BIOS shadow status
70h		Display error messages
72h		Check for configuration errors
76h		Check for keyboard errors
7Ch		Set up hardware interrupt vectors
7Dh		Initialilze Intelligent System Monitoring
7Eh		Initialize coprocessor if present
80h		Disable onboard Super I/O ports and IRQs
81h		Late POST device initialisation
82h		Detect and install external RS232 ports
83h		Configure non-MCD IDE controllers
84h		Detect and install external parallel ports
85h		Initialize PC-compatible PnP ISA devices
86h		Re-initialize onboard I/O ports.
87h		Configure Motheboard Configurable Devices (optional)
88h		Initialize BIOS Data Area
89h		Enable Non-Maskable Interrupts (NMIs)
8Ah		Initialize Extended BIOS Data Area
8Bh		Test and initialize PS/2 mouse
8Ch		Initialize floppy controller
8Fh		Determine number of ATA drives (optional)
90h		Initialize hard-disk controllers
91h		Program timing registers according to PIO modes
92h		Jump to UserPatch2
93h		Build MPTABLE for multi-processor boards
95h		Install CD ROM for boot
96h		Clear huge ES segment register
97h		Fixup Multi Processor table
98h	1-2	Enable PCI devices and ROM Scan One long, two short beeps on checksum failure
99h		Check for SMART Drive
9Ah		Shadow option ROMs
9Ch		Set up Power Management
9Dh		Initialize security engine (optional)
9Eh		Enable hardware interrupts
9Fh		Determine number of ATA and SCSI drives
A0h		initialize IGD Graphics Device, initialize MRC Parameter Frame
A2h		Check key lock
A4h		Initialize typematic rate
A8h		Erase F2 prompt
AAh		Scan for F2 key stroke
ACh		Enter SETUP
AEh		Clear Boot flag
B0h		Check for errors
B1h		Inform RomPilot about the end of POST.
B2h		POST done - prepare to boot operating system
B3h		store enhanced CMOS values in non-volatile area
B4h		1 One short beep before boot
B5h		Terminate QuietBoot (optional)
B6h		Check password (optional)

Code	Beeps	POST Task Description
B7h		Initialize ACPI BIOS
B9h		Prepare Boot
BAh		Initialize DMI parameters
BCh		Clear parity checkers
BDh		Display MultiBoot menu
BEh		Clear screen (optional)
BFh		Check virus and backup reminders
C0h		Try to boot with INT 19
C1h		Initialize POST PEM Error Manager
C2h		Initialize PEM error logging
C3h		Initialize error PEM display function
C4h		Initialize PEM system error handler
C5h		PnPnd dual CMOS (optional)
C6h		Initialize note dock (optional)
C7h		Initialize note dock late
C8h		Force check (optional)
C9h		Extended checksum (optional)
CAh		Redirect Int 15h to enable remote keyboard
CBh		Redirect Int 13h to Memory Technologies
CCh		Redirect Int 10h to enable remote serial video
CDh		Remap I/O and memory for PCMCIA
CEh		Initialize digitizer and display message
D2h		Unknown interrupt or exception
E0h		DIMM Type Detection Error
E1h		Memory Configuration Error

5.6.3 Memory Detection Postcodes

Code	Calistoga Memory Detection
FFA0h	Start memory detection
FF01h	Enable MCHBAR
FF02h	Check for DRAM initialisation interrupt and reset fail
FF03h	Verify all DIMMs are DDR2 and unbuffered
FF04h	Detect an improper warm reset and handle
FF05h	Detect if ECC SO-DIMMs are present in the system
FF06h	Verify all DIMMs are single or double sided and not asymmetric
FF07h	Verify all DIMMs are x8 or x16 width
FF08h	Find a common CAS latency between the DIMMS and the MCH
FF09h	Determine the memory frequency and CAS latency to program
FF10h	Determine the smallest common TRAS for all DIMMs
FF11h	Determine the smallest common TRP for all DIMMs
FF12h	Determine the smallest common TRCD for all DIMMs
FF13h	Determine the smallest refresh period for all DIMMs
FF14h	Verify burst length of 8 is supported by all DIMMs
FF15h	Determine the smallest tWR supported by all DIMMs
FF16h	Determine DIMM size parameters
FF17h	Program Graphics frequency and PLL settings
FF18h	Program system memory frequency
FF19h	Determine and set the mode of operation for the memory channels
FF20h	Program clock crossing registers
FF21h	Disable Fast Dispatch
FF22h	Program the DRAM Row Attributes and DRAM Row Boundary registers
FF23h	Program the DRAM Bank Architecture register
FF24h	Program the DRAM Timing & and DRAM Control registers
FF25h	Program ODT
FF26h	Perform steps required before memory init
FF27h	Program the receive enable reference timing control register Program the DLL Timing Control Registers , RCOMP settings
FF28h	Enable DRAM Channel I/O Buffers
FF29h	Enable all clocks on populated rows
FF30h	Perform JEDEC memory initialization for all memory rows
FF31h	Program PM Settings
FF32h	Perform additional steps required after memory init
FF33h	Program DRAM throttling and throttling event registers
FF34h	Setup DRAM control register for normal operation and enable
FF35h	Setup DRAM control register for normal operation and enable
FF36h	Enable RCOMP
FF37h	Clear DRAM initialization bit in the ICH

5.6.4 ACPI Postcodes

Code	ACPI Codes
03h	Enter Suspend State S3
04h	Enter Hibernate State S4
05h	Enter Softoff State S5
ABh	Enter Wakeup from Powerstate
CDh	End Wakeup from Powerstate