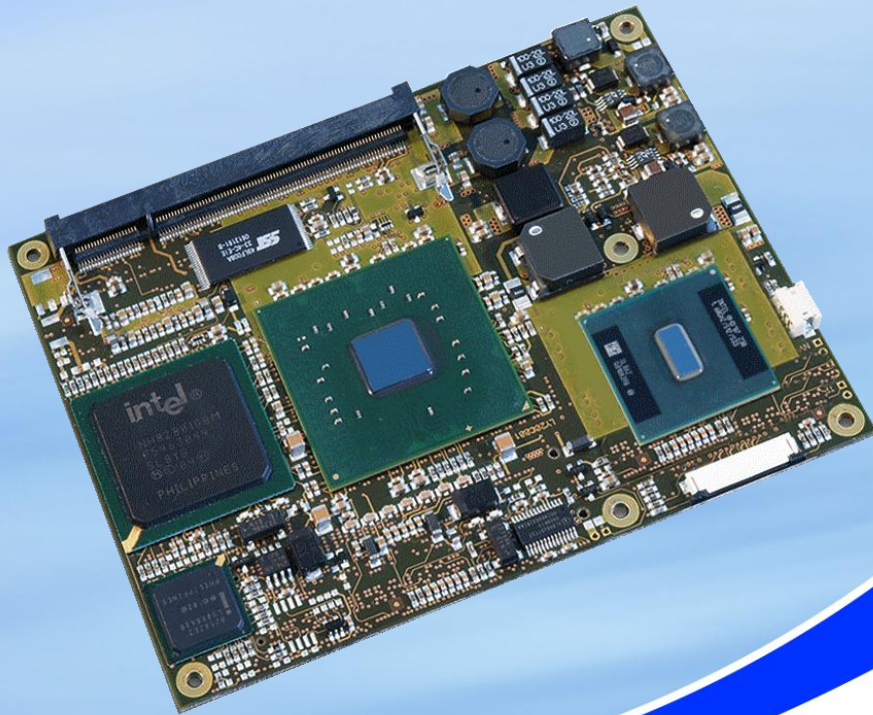


User's Manual



CXB-A945M

MSC COM Express™ Basic Module

Rev. 1.3
May 6th, 2010



MICROCOMPUTERS · SYSTEMS · COMPONENTS · VERTRIEBS GMBH

... embedding excellence

Preface

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1 General Information

1.1 Revision History

| Rev. | Date | Description |
|------|---------------------------------|--|
| 1.0 | March, 03 rd 2009 | Release Version |
| 1.1 | December, 11 th 2009 | SYS_RESET# description corrected. Bios Setup corrections (depending on Bios V2.20). |
| 1.2 | Februar, 8 th 2010 | Updated PCI Resource Table |
| 1.3 | May, 6 th 2010 | Minor fixes |

1.2 Reference Documents

- [1] COM Express Module Base Specification
COM Express Revision 1.0
Last update: July 10th, 2005
- [2] PCI Local Bus Specification Rev. 2.1
PCI21.PDF
Last update: June 1st, 1995
<http://www.pcisig.com>
- [3] ATA/ATAPI-6 Specification
d1410r3b.pdf
<http://www.t13.org/>
- [4] Serial ATA Specification
Serial ATA 1.0 gold.pdf
Last update: August 29th, 2002 Rev.1.0
<http://www.sata-io.org/>
- [5] IEEE Std. 802.3-2002
802.3-2002.pdf
<http://www.ieee.org>
- [6] Universal Bus Specification
usb_20.pdf
Last update: April 27th, 2000
<http://www.usb.org>
- [7] COM Express Carrier Design Guide Rev. 1.0
Last update: March 13, 2009
<http://www.picmg.org>

1.3 Introduction

COM Express™, an open specification from PICMG (PCI Industrial Computer Manufacturer Group), is a module concept to bring PCI Express and other new technologies such as SATA, USB 2.0 and LVDS onto a COM (Computer On Module).

Typically a COM Express module consists of CPU, chipset, memory, video controller, Ethernet controller, BIOS flash and EIDE-, SATA- and USB controller. Interface controllers (e.g. for PCMCIA) or connectors (e.g. RJ45) are implemented on the base board on to which the COM Express module can be mounted via one or two 220-pin SMD-connectors. In addition to the power supply signals for PCIe-, PCI-bus, EIDE, SATA, USB, LPC etc. are also present on these connectors.

A COM Express™ module is plugged into an application-specific base board in a similar manner to the ETX concept, but offering more options and a growth path to future CPU technologies. Utilizing different sizes, COM Express™ can be used in a range of applications from highly embedded solutions up to high performance platforms.

The design of the MSC CXB-A945M module combines the low power technology of the Intel® Atom™ Processor (Diamondville) together with the high graphics performance of the Intel® 945GME chipset and the advanced I/O capability of the Intel® ICH7-M/DH. Thus enabling customers to boost their embedded application performance levels while consuming less power.

For evaluation and design-in of the COM Express™ modules MSC offers evaluation and development baseboards providing the I/O infrastructure for the COM Express™ module based on PC type interfaces.

Currently two module sizes are defined in the COM Express Specification 1.0: the Basic Module and the Extended Module. In addition MSC and other manufacturers have created a third smaller form factor the "Compact" Module. The primary difference between the Compact, the Basic and the Extended Module is the over-all physical size and the performance envelope supported by each. The Extended Module is the largest and can support larger processor and memory solutions. The Basic Module is the most common supporting typical processor platforms in the embedded world. The Compact format allows smaller and more portable system solutions. All module sizes use the same connectors and pin-outs and utilize several common mounting hole positions. This level of compatibility allows that a carrier board designed to accommodate an Extended Module can also support a Basic or a Compact Module.

Up to 440 pins of connectivity are available between COM Express™ modules and the Carrier Board. Legacy buses such as PCI, parallel ATA, LPC are supported as well as new high speed serial interconnects such as PCI Express, Serial ATA and Gigabit Ethernet.

To enhance interoperability between COM Express™ modules and Carrier Boards, five common signalling configurations (Pin-out Types) have been defined to ease system integration.

2 Technical Description

2.1 **Key Features**

The MSC CXB-A945M COM Express module is designed as a type 2 module.

Key features include:

Module size: 125 mm x 95 mm

18 mm 'z' height with heat-spreader (with 5 mm baseboard connector option)

Dual 220 pin (440 pins) COM Express connector

1x DDR2 SO-DIMM module

Eight USB 2.0 ports; 4 shared over-current signals

Two Serial ATA ports

Five PCI Express x1 lanes

Support signals for one ExpressCard

One dual channel 24-bit LVDS display interface

Analog VGA

AC '97 / High definition digital audio interface (external CODEC)

Single GigaBit Ethernet interface

LPC interface

Four GPI pins

Four GPO pins

+12V primary power supply input

+5V standby (optional) and 3.3V RTC power supply inputs

32 bit PCI interface

IDE port (to support legacy ATA devices such as CD-ROM drives and Compact Flash storage cards)

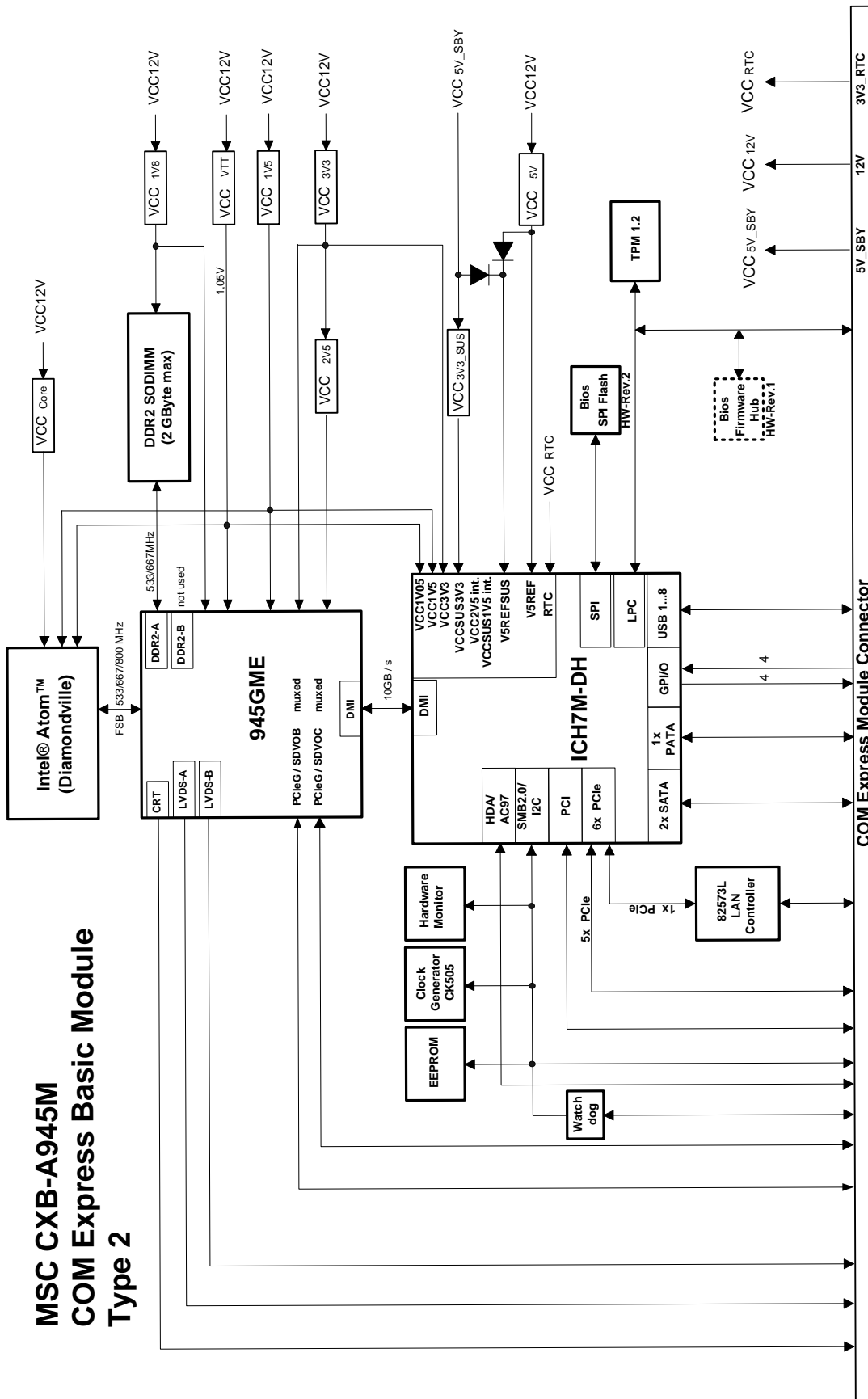
21 PCI Express lanes (5 on A-B and 16 on C-D)

16 of 21 PCI Express lanes can be used for external PCI Express Graphics

Two SDVO ports (pins multiplexed with PCI Express Graphics)

TPM module (option, TPM 1.2, SLB9635)

2.2 Block Diagram



2.3 COM Express Implementation

COM Express™ required and optional features for pin-out type 2 are summarized in the following table. The features identified as Minimum (Min.) **shall** be implemented by all modules. Features identified up to Maximum (Max) **may** be additionally implemented by a module.

The column MSC CXB-A945M shows the implemented features of the MSC module:

| | Type 2 | MSC CXB-A945M | Note |
|--|-----------|---------------|---|
| | Min / Max | | |
| System I/O | | | |
| PCI Express Graphics (PEG) | 0 / 1 | 1 | signals are multiplexed with SDVO signals |
| PCI Express Lanes 0 - 5 | 2 / 6 | 5 (x1) | lane 6 is reserved for GigaBit LAN |
| PCI Express Lanes 16-31 (same as PEG pins) | 0 / 16 | 1 (x16) | off-module x16 PCI Express Graphics |
| SDVO Channels | 0 / 2 | 2 | signals are multiplexed with PEG signals |
| LVDS Channels | 0 / 2 | 2 | 1x dual channel, 2x24 Bit |
| VGA Port | 0 / 1 | 1 | |
| TV-Out | 0 / 1 | 0 | not implemented |
| PATA Port | 1 / 1 | 1 | |
| SATA Ports | 2 / 4 | 2 | |
| AC'97 / HDA Digital Interface | 0 / 1 | 1 | AC97 or High Definition Audio |
| USB 2.0 Ports | 4 / 8 | 8 | |
| Gbit LAN | 1 / 1 | 1 | |
| PCI Bus - 32 Bit | 1 / 1 | 1 | |
| Express Card Support | 1 / 2 | 1 | |
| LPC Bus | 1 / 1 | 1 | |
| System Management | | | |
| General Purpose Inputs | 4 / 4 | 4 | |
| General Purpose Outputs | 4 / 4 | 4 | |
| SMBus | 1 / 1 | 1 | |
| I2C | 1 / 1 | 1 | |
| Watch Dog Timer | 0 / 1 | 1 | |
| Speaker Out | 1 / 1 | 1 | |
| External BIOS ROM support | 0 / 1 | 1 | |
| Reset Functions | 1 / 1 | 1 | |
| Power Management | | | |
| Thermal Protection | 0 / 1 | 1 | |
| Battery Low Alarm | 0 / 1 | 1 | |
| Suspend | 0 / 1 | 1 | |
| Wake | 0 / 2 | 2 | |
| Power Button Support | 1 / 1 | 1 | |
| Power Good | 1 / 1 | 1 | |
| TPM | 0 / 0 | 1 | optional TPM 1.2 module |

2.4 Functional Units

| | |
|------------------------------|---|
| CPU | Intel® Atom™ N270 Processor (Diamondville, 1.6 GHz, FSB 533MHz, 437 pins FCBGA8) |
| Chipset | Intel® 82945GME GMCH (Graphics Memory Controller Hub) Intel® ICH7-M/DH I/O Controller Hub |
| Memory | 200-pin DDR2 SO-DIMM socket for up to 2GB (max. height: 1250 mil = 31.75 mm) PC5300 DDR2 SDRAM (DDR400/533/667) |
| SATA | 2 SATA channels up to 150MB/s each |
| EIDE | 1 Enhanced IDE port ATA/UDMA100 |
| USB | 8 x USB 2.0 |
| COM Express™ | Type 2 interface, fully compliant |
| PCI Express™ | 5 channels PCIe x1 |
| PCI | 32 Bit standard interface |
| LPC | Low Pin Count Bus for heritage interfaces |
| Graphics Controller | Intel® Graphics Media Accelerator 950 (integrated in Intel® 945GME chipset) |
| Video Memory | UMA, up to 224 MB |
| LCD Interface | LVDS 2x24Bit, dual channel, max. resolution 1600 x 1200 |
| SDVO Interface | 2 independent SDVO interfaces (SDVOB, SDVOC) or external PCIe x16 graphics (multiplexed with Intel® Graphics Media Accelerator 950) |
| CRT Interface | Max. resolution 2048 x 1536 |
| Ethernet | 10/100/1000Base-TX (Intel® 82573L) |
| Sound Interface | AC97 or High Definition Audio Interface |
| Watchdog Timer | PIC12C509A Creates system reset (programmable, 1s ... 255h) |
| TPM (option) | Optional Trusted Platform Module, TPM 1.2, SLB9635 |
| Fan Supply | 3-pin header (12V) |
| Real Time Clock (RTC) | Integrated in ICH7-M/DH |
| Battery | External on carrier board |
| System Monitoring | Voltage, Temperature , Fan CPU Core voltage 12V 5V_SBY CPU thermal diode CPU Fan Speed |

2.5 Power Supply

- **+12V primary power supply input**
- **+5V standby**
 Optional, is not required for module operation.
 If not present, customer has to ensure that the supply voltages which are generated on the carrier board are switched off during suspend states, so that no current from the carrier board's signal lines can flow to the CPU board.
- **3.3V RTC power supply**
 Option, is not required for module operation.
 BIOS SETUP data is stored in a non volatile backup memory device (EEPROM), therefore configuration data will not get lost during power off (except for time and date information)

| Voltage | Input range | Current |
|----------------------|-----------------|---------------------|
| +12V | +11.4V - 12.6 V | See next table |
| +5V Standby | +4.75V - 5.25 V | 115 mA (during STR) |
| +3V RTC power supply | +2.0V - 3.3V | max. 6µA |

2.6 Module Power Dissipation

DOS Prompt, 512MB DDR2 SO-DIMM

| Module (CPU) | Voltage | Current (typ.) |
|---|---------|----------------|
| Intel® Atom™ N270 Processor (Diamondville,1.60 GHz) | +12V | 775 mA |

Windows XP, Intel TAT! Tool, 100% Workload, 512MB DDR2 SO-DIMM

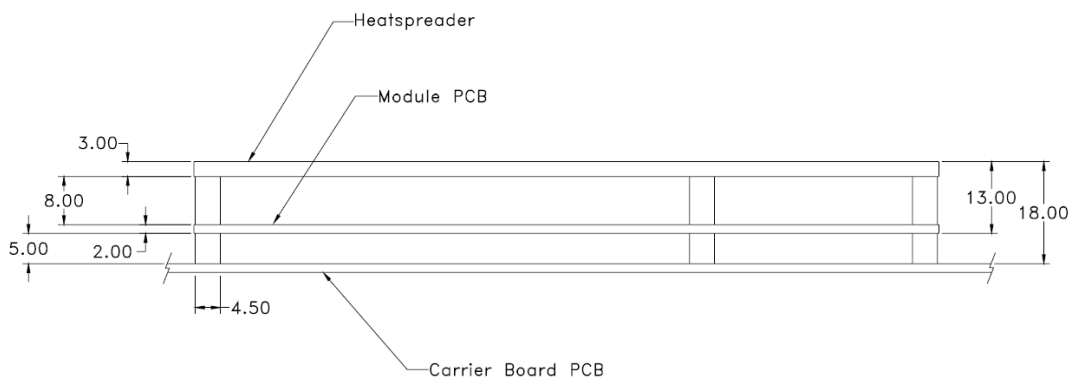
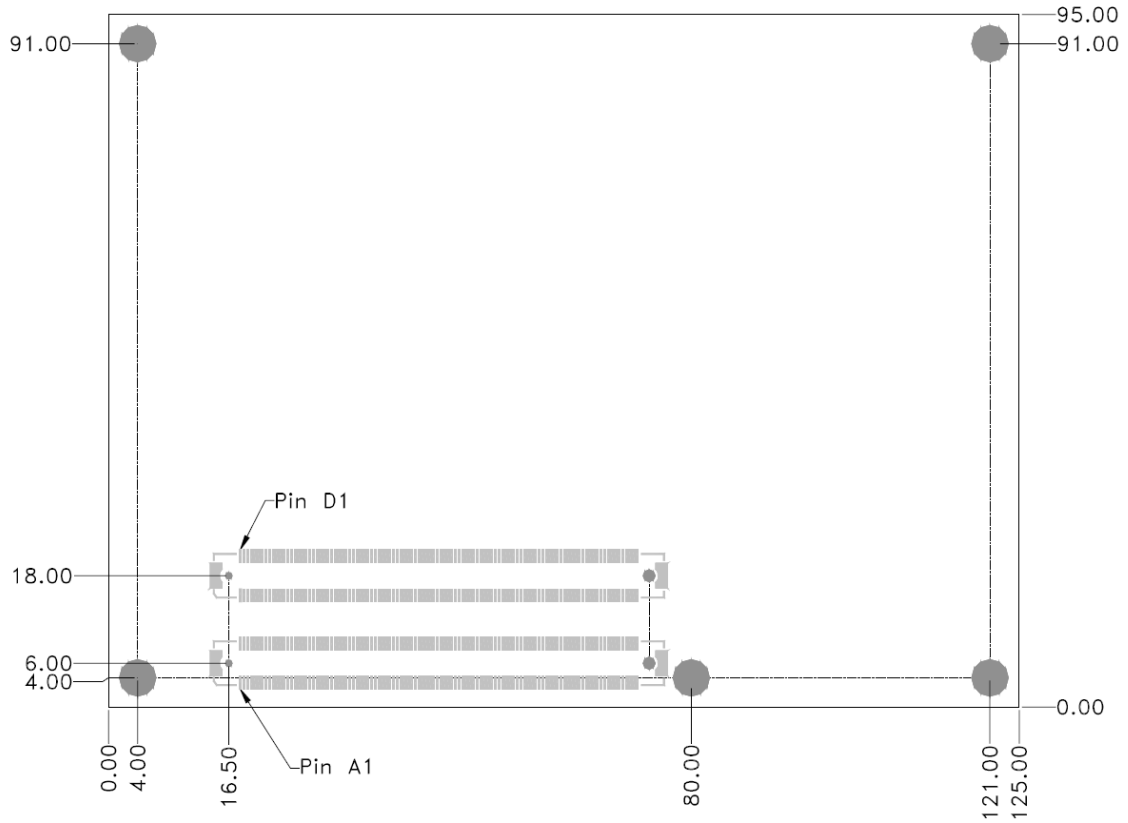
| Module (CPU) | Voltage | Current (typ.) |
|---|---------|----------------|
| Intel® Atom™ N270 Processor (Diamondville,1.60 GHz) | +12V | 900 mA |

2.7 Mechanical Dimensions

2.7.1 Basic Module

There are two height options defined in the COM Express specification, 5mm and 8mm.

The height option is defined by the connectors on the baseboard.



2.8 Thermal Specifications

The cooling solution for a COM Express module is based on a heatspreader concept.

A heatspreader is a metal plate (typically aluminium) mounted on the top of the module. The connection between this plate and the module components is typically done by thermal interface materials such as phase change foils, gap pads and copper or aluminium blocks. A very good thermal contact is required in order to conduct the heat away from the CPU and chipset to the heatspreader plate.

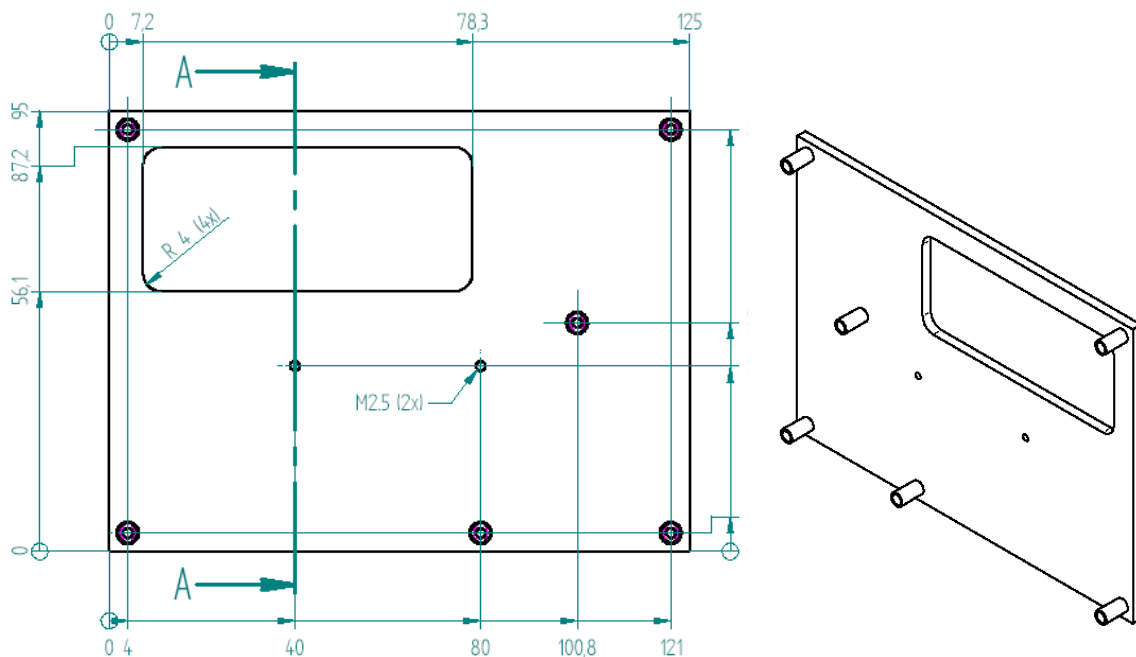
The heatspreader for the MSC module is thermally attached using phase change material and small aluminium blocks filling the space between CPU and chipset dies and the heatspreader plate.

The heatspreader is however not a heatsink!

It is a defined thermal interface for the system designer with fixed mechanical dimensions, so making it possible to swap different module types without problem. There must be some form of cooling solution for the system so that the surface temperature of the heatspreader does not exceed 60°C .

The main criterion for the thermal functionality of the system is that each device on the module is operated within its specified thermal values. The maximum value for the CPU is 90°C and for the chipset is 100°C. So there may be system implementations where the heatspreader temperature could be higher.

In this case it has to be validated that there are no violations of the thermal specification of any assembled part or integrated circuit over the system temperature range even under worst case conditions.



2.9 Signal Description

In the following tables signals are marked with the power rail associated with that pin, and for I/O pins, with the input voltage tolerance (3.3V or 5V). The signal power rail and the pin input voltage tolerance **may** be different. For example, the PCI group is defined as having a 3.3V power rail, meaning that the output signals will only be driven to 3.3V, but the pins are 5V tolerant .

An additional label “Suspend”, indicates that the pin is active during suspend states (S3, S4, S5). If suspend modes are used, then care must be taken to avoid loading signals that are active during suspend to avoid excessive suspend mode current draw.

2.9.1 AC97 Audio / High Definition Audio

| Signal | Pin Type | Signal Level | Power Rail | Voltage Tolerance | PU/PD | Description | Source / Target |
|--------------|------------------|--------------|--------------|-------------------|--------|--|-----------------|
| AC_RST# | Output | CMOS | 3.3V Sus. | 3.3V | | Reset output to CODEC, active low. | ICH7-M/DH |
| AC_SYNC | Output | CMOS | 3.3V | 3.3V | | 48kHz fixed-rate, sample-synchronization signal to the CODEC(s). | ICH7-M/DH |
| AC_BITCLK | Input/ Output | CMOS | 3.3V | 3.3V | | AC97: 12.228 MHz serial data clock generated by the external CODEC(s). HDA: 24.00 MHz serial data clock generated by the ICH7-M | ICH7-M/DH |
| AC_SDOUT | Output | CMOS | 3.3V | 3.3V | | Serial TDM data output to the CODEC. | ICH7-M/DH |
| AC_SDIN[0:2] | Input | CMOS | 3.3V Sus. | 3.3V | 20k PD | Serial TDM data inputs from up to 3 CODECs. | ICH7-M/DH |

2.9.2 Ethernet

| Signal | Pin Type | Signal Level | Power Rail | Voltage Tolerance | PU/PD | Description | Source / Target |
|----------------------------------|------------------|--------------|--------------|-------------------|-------|--|-----------------|
| GBE0_MDI[0:3]+ GBE0_MDI[0:3]- | Input/ Output | Analog | 3.3V Sus. | | | Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. MDI[0]+/- B1_DA+/- MDI[1]+/- B1_DB+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/- | 82573L |
| GBE0_ACT# | Open Drain | CMOS | 3.3V Sus. | 3.3V | | Gigabit Ethernet Controller 0 activity indicator, active low. | 82573L |
| GBE0_LINK# | Open Drain | CMOS | 3.3V Sus. | 3.3V | | Gigabit Ethernet Controller 0 link indicator, active low. | 82573L |
| GBE0_LINK100# | Open Drain | CMOS | 3.3V Sus. | 3.3V | | Gigabit Ethernet Controller 0 100 Mbit/sec link indicator, active low. | 82573L |

| Signal | Pin Type | Signal Level | Power Rail | Voltage Tolerance | PU/PD | Description | Source / Target |
|----------------|------------|--------------|------------|---------------------|-------|--|-----------------|
| GBE0_LINK1000# | Open Drain | CMOS | 3.3V Sus. | 3.3V | | Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low. | 82573L |
| GBE0_CTREF | REF | | Sus. | GND min 3.3V max | | Gigabit Ethernet Controller 0 center tab reference voltage for LAN magnetics, 2.5V | 82573L |

2.9.3 IDE

| Signal | Pin Type | Signal Level | Power Rail | Voltage Tolerance | PU/PD | Description | Source / Target |
|----------------------------|----------|--------------|------------|-------------------|--------|---|-------------------|
| IDE_D[0:6], IDE_D[8:15] | I/O | CMOS | 3.3V | 5V | | Bidirectional data to / from IDE device. | ICH7-M/DH |
| IDE_D[7] | I/O | CMOS | 3.3V | 5V | 12k PD | Bidirectional data to / from IDE device. | ICH7-M/DH |
| IDE_A[0:2] | O | CMOS | 3.3V | 3.3V | | Address lines to IDE device. | ICH7-M/DH |
| IDE_IOW# | O | CMOS | 3.3V | 3.3V | | I/O write line to IDE device. Data latched on trailing (rising) edge. | ICH7-M/DH |
| IDE_IOR# | O | CMOS | 3.3V | 3.3V | | I/O read line to IDE device. | ICH7-M/DH |
| IDE_REQ | I | CMOS | 3.3V | 5V | 12k PD | IDE Device DMA Request. It is asserted by the IDE device to request a data transfer. | ICH7-M/DH |
| IDE_ACK# | O | CMOS | 3.3V | 3.3V | | IDE Device DMA Acknowledge. | ICH7-M/DH |
| IDE_CS1# | O | CMOS | 3.3V | 3.3V | | IDE Device Chip Select for 1F0h to 1FFh range. | ICH7-M/DH |
| IDE_CS3# | O | CMOS | 3.3V | 3.3V | | IDE Device Chip Select for 3F0h to 3FFh range. | ICH7-M/DH |
| IDE_IORDY | I | CMOS | 3.3V | 5V | 4k7 PU | IDE device I/O ready input. Pulled low by the IDE device to extend the cycle. | ICH7-M/DH |
| IDE_RESET# | O | CMOS | 3.3V | 3.3V | | Reset output to IDE device, active low. | ICH7-M/DH |
| IDE_IRQ | I | CMOS | 3.3V | 5V | 8k2 PU | Interrupt request from IDE device. | ICH7-M/DH |
| IDE_CBLID# | I | CMOS | 3.3V | 5V | 10K PD | Input from off-module hardware indicating the type of IDE cable being used. High indicates a 40-pin cable used for legacy IDE modes. Low indicates that an 80-pin cable with interleaved grounds is used. Such a cable is required for Ultra-DMA 66, 100 and 133 modes. | ICH7-M/DH / GPIO4 |

2.9.4 Serial ATA

| Signal | Pin Type | Signal Level | Power Rail | Remark | PU/PD | Description | Source / Target |
|------------------------|----------------|--------------|------------|----------------------|-------|--|-----------------|
| SATA0_TX+ SATA0_TX- | O | SATA | 3.3V | AC coupled on module | | Serial ATA Channel 0 Transmit Differential Pair. | ICH7-M/DH |
| SATA0_RX+ SATA0_RX- | I | SATA | 3.3V | AC coupled on module | | Serial ATA Channel 0 Receive Differential Pair. | ICH7-M/DH |
| SATA1_TX+ SATA1_TX- | O | SATA | 3.3V | AC coupled on module | | Serial ATA Channel 1 Transmit Differential Pair. | not supported |
| SATA1_RX+ SATA1_RX- | I | SATA | 3.3V | AC coupled on module | | Serial ATA Channel 1 Receive Differential Pair. | not supported |
| SATA2_TX+ SATA2_TX- | O | SATA | 3.3V | AC coupled on module | | Serial ATA Channel 2 Transmit Differential Pair. | ICH7-M/DH |
| SATA2_RX+ SATA2_RX- | I | SATA | 3.3V | AC coupled on module | | Serial ATA Channel 2 Receive Differential Pair. | ICH7-M/DH |
| SATA3_TX+ SATA3_TX- | O | SATA | 3.3V | AC coupled on module | | Serial ATA Channel 3 Transmit differential Pair. | not supported |
| SATA3_RX+ SATA3_RX- | I | SATA | 3.3V | AC coupled on module | | Serial ATA Channel 3 Receive Differential Pair. | not supported |
| SATA_ACT# | Open Collector | CMOS | 3.3V | 3.3V | | Serial ATA Activity Indicator, active low, 6mA. This signal has an internal pullup in a range from 10 kΩ to 20 kΩ that is only enabled only during CB_RESET# assertion. Do not pull low. | ICH7-M/DH |

2.9.5 PCI Express Lanes

| Signal | Pin Type | Signal Level | Power Rail | Remark / Volt. Tol. | PU/PD | Description | Source / Target |
|--------------------------------|----------|--------------|------------|-----------------------|-------|---|-----------------|
| PCIE_TX[0:4]+ PCIE_TX[0:4]- | O | PCIe | 3.3V | AC coupled on module | | PCI Express Differential Transmit Pairs 0 through 4. | ICH7-M/DH |
| PCIE_RX[0:4]+ PCIE_RX[0:4]- | I | PCIe | 3.3V | AC coupled off module | | PCI Express Differential Receive Pairs 0 through 4. | ICH7-M/DH |
| PCIE_TX[5]+ PCIE_TX[5]- | O | PCIe | 3.3V | AC coupled on module | | PCI Express Differential Transmit Pair 5. (Reserved for on-module Gigabit Ethernet controller). | not supported |

| Signal | Pin Type | Signal Level | Power Rail | Remark / Volt. Tol. | PU/PD | Description | Source / Target |
|------------------------------------|----------|--------------|------------|--------------------------|-------|--|-----------------|
| PCIE_RX[5]+ PCIE_RX[5]- | I | PCIe | 3.3V | AC coupled off module | | PCI Express Differential Receive Pair 5. (Reserved for on-module Gigabit Ethernet controller). | not supported |
| PCIE_TX[16:31]+ PCIE_TX[16:31]- | O | PCIe | 3.3V | AC coupled on module | | PCI Express Differential Transmit Pairs 16 through 31. These are same lines as PEG_TX[0:15]+ and - in module pin-out types 4 and 5.(| 945GME |
| PCIE_RX[16:31]+ PCIE_RX[16:31]- | I | PCIe | 3.3V | AC coupled off module | | PCI Express Differential Receive Pairs 16 through 31. These are the same lines as PEG_RX[0:15]+ and - in module pin-out types 4 and 5. | 945GME |
| PCIE_CLK_REF+ PCIE_CLK_REF- | O | PCIe CLK | 3.3V | AC coupled on module | | Reference clock output for all PCI Express and PCI Express Graphics lanes. | ICS9LPRS365 |

2.9.6 PCI Express Lanes x16

| Signal | Pin Type | Signal Level | Power Rail | Remark / Volt. Tol. | PU/PD | Description | Source / Target |
|--------------------------------|----------|--------------|------------|--------------------------|--------|--|---------------------|
| PEG_TX[0:15]+ PEG_TX[0:15]- | O | PCIe | 3.3V | AC coupled on module | | PCI Express Graphics transmit differential pairs. Some of these are multiplexed with SDVO lines (see SDVO section). These are the same lines as PCIE_TX[16:31]+ and - in module pin-out types 4 and 5. | 945GME |
| PEG_RX[0:15]+ PEG_RX[0:15]- | I | PCIe | 3.3V | AC coupled off module | | PCI Express Graphics receive differential pairs. Some of these are multiplexed with SDVO lines (see SDVO section). These are the same lines as PCIE_RX[16:31]+ and - in module pin-out types 4 and 5. | 945GME |
| PEG_LANE_RV# | I | CMOS | 3.3V | 3.3V | 5k7 PU | PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order. Be aware that the SDVO lines that share this interface do also reverse lane order if this strap is low. | 945GME (CFG 9) |
| PEG_ENABLE# | I | CMOS | 3.3V | 3.3V | 8k2 PU | Strap to enable PCI Express x16 external graphics interface. Pull low to disable internal graphics and enable the x16 interface. | ICH7-M/DH (GPI3) |

2.9.7 Express Card Support

| Signal | Pin Type | Signal Level | Power Rail | Remark / Volt. Tol. | PU/PD | Description | Source / Target |
|---------------|----------|--------------|------------|---------------------|--------|--------------------------------------|-----------------|
| EXCD[0]_CPPE# | I | CMOS | 3.3V | 3.3V | 8k2 PU | ExpressCard card request, active low | ICH7-M/DH |
| EXCD[1]_CPPE# | I | CMOS | 3.3V | 3.3V | | ExpressCard card request, active low | Not supported |

| Signal | Pin Type | Signal Level | Power Rail | Remark / Volt. Tol. | PU/PD | Description | Source / Target |
|--------------|----------|--------------|------------|---------------------|--------|-------------------------------|-----------------|
| EXCD[0]_RST# | O | CMOS | 3.3V | 3.3V | 8k2 PU | ExpressCard reset, active low | ICH7-M/DH |
| EXCD[1]_RST# | O | CMOS | 3.3V | 3.3V | 8k2 PU | ExpressCard reset, active low | Not supported |

2.9.8 PCI Bus

| Signal | Pin Type | Signal Level | Power Rail | Remark / Volt. Tol. | PU/PD | Description | Source / Target |
|----------------|-----------|--------------|------------|---------------------|--------|--|-----------------|
| PCI_AD[0:31] | I/O | CMOS | 3.3V | 5V | | PCI bus multiplexed address and data lines | ICH7-M/DH |
| PCI_C/BE[0:3]# | I/O | CMOS | 3.3V | 5V | | PCI bus byte enable lines, active low | ICH7-M/DH |
| PCI_DEVSEL# | I/O | CMOS | 3.3V | 5V | 8k2 PU | PCI bus Device Select, active low. | ICH7-M/DH |
| PCI_FRAME# | I/O | CMOS | 3.3V | 5V | 8k2 PU | PCI bus Frame control line, active low. | ICH7-M/DH |
| PCI_IRDY# | I/O | CMOS | 3.3V | 5V | 8k2 PU | PCI bus Initiator Ready control line, active low. | ICH7-M/DH |
| PCI_TRDY# | I/O | CMOS | 3.3V | 5V | 8k2 PU | PCI bus Target Ready control line, active low. | ICH7-M/DH |
| PCI_STOP# | I/O | CMOS | 3.3V | 5V | 8k2 PU | PCI bus STOP control line, active low, driven by cycle initiator. | ICH7-M/DH |
| PCI_PAR | I/O | CMOS | 3.3V | 5V | | PCI bus parity | ICH7-M/DH |
| PCI_PERR# | I/O | CMOS | 3.3V | 5V | 8k2 PU | Parity Error: An external PCI device drives PERR# when it receives data that has a parity error. | ICH7-M/DH |
| PCI_REQ[0:3]# | I | CMOS | 3.3V | 5V | 8k2 PU | PCI bus master request input lines, active low. | ICH7-M/DH |
| PCI_GNT[0:3]# | O | CMOS | 3.3V | 5V | | PCI bus master grant output lines, active low. | ICH7-M/DH |
| PCI_RESET# | O | CMOS | 3.3V Sus. | 5V | | PCI Reset output, active low. | ICH7-M/DH |
| PCI_LOCK# | I/O | CMOS | 3.3V | 5V | 8k2 PU | PCI Lock control line, active low. | ICH7-M/DH |
| PCI_SERR# | I/O OD | CMOS | 3.3V | 5V | 8k2 PU | System Error: SERR# may be pulsed active by any PCI device that detects a system error condition. | ICH7-M/DH |
| PCI_PME# | I | CMOS | 3.3V Sus. | 5V | 20k PU | PCI Power Management Event: PCI peripherals drive PME# to wake system from low-power states S1–S5. | ICH7-M/DH |
| PCI_CLKRUN# | I/O | CMOS | 3.3V | 5V | 8k2 PU | Bidirectional pin used to support PCI clock run protocol for mobile systems. | ICH7-M/DH |
| PCI_IRQ[A:D]# | I | CMOS | 3.3V | 5V | 8k2 PU | PCI interrupt request lines. | ICH7-M/DH |
| PCI_CLK | O | CMOS | 3.3V | 3.3V | | PCI 33MHz clock output. | ICS9LPRS3 65 |

| Signal | Pin Type | Signal Level | Power Rail | Remark / Volt. Tol. | PU/PD | Description | Source / Target |
|-----------|----------|--------------|------------|---------------------|-------|--|-----------------|
| PCI_M66EN | I | CMOS | 3.3V | 5V | | <p>Module input signal indicates whether an off-module PCI device is capable of 66MHz operation. Pulled to GND by Carrier Board device or by Slot Card if the devices are NOT capable of 66 MHz operation.</p> <p>If the module is not capable of supporting 66 MHz PCI operation, this input may be a no-connect on the module.</p> <p>If the module is capable of supporting 66 MHz PCI operation, and if this input is held low by the Carrier Board, the module PCI interface shall operate at 33 MHz.</p> | Not supported |

2.9.9 USB

| Signal | Pin Type | Signal Level | Power Rail | Remark / Volt. Tol. | PU/PD | Description | Source / Target |
|------------------------|----------|--------------|------------|---------------------|--------|--|-----------------|
| USB[0:7]+ USB[0:7]- | I/O | USB | 3.3V Sus. | 3.3V | | USB differential pairs, channels 0 through 7 | ICH7-M/DH |
| USB_0_1_OC# | I | CMOS | 3.3V Sus. | 3.3V | 8k2 PU | <p>USB over-current sense, USB channels 0 and 1. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low.</p> <p>Do not pull this line high on the Carrier Board.</p> | ICH7-M/DH |
| USB_2_3_OC# | I | CMOS | 3.3V Sus. | 3.3V | 8k2 PU | <p>USB over-current sense, USB channels 2 and 3. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low.</p> <p>Do not pull this line high on the Carrier Board.</p> | ICH7-M/DH |
| USB_4_5_OC# | I | CMOS | 3.3V Sus. | 3.3V | 8k2 PU | <p>USB over-current sense, USB channels 4 and 5. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low.</p> <p>Do not pull this line high on the Carrier Board.</p> | ICH7-M/DH |
| USB_6_7_OC# | I | CMOS | 3.3V Sus. | 3.3V | 8k2 PU | <p>USB over-current sense, USB channels 6 and 7. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low.</p> <p>Do not pull this line high on the Carrier Board.</p> | ICH7-M/DH |

2.9.10 LVDS Flat Panel

| Signal | Pin Type | Signal Level | Power Rail | Remark / Volt. Tol. | PU/PD | Description | Source / Target |
|------------------------------|-----------|--------------|------------|---------------------|---------|---|-----------------|
| LVDS_A[0:3]+ LVDS_A[0:3]- | O | LVDS | | | | LVDS Channel A differential pairs | 945GME |
| LVDS_A_CK+ LVDS_A_CK- | O | LVDS | | | | LVDS Channel A differential clock | 945GME |
| LVDS_B[0:3]+ LVDS_B[0:3]- | O | LVDS | | | | LVDS Channel B differential pairs | 945GME |
| LVDS_B_CK+ LVDS_B_CK- | O | LVDS | | | | LVDS Channel B differential clock | 945GME |
| LVDS_VDD_EN | O | CMOS | 3.3V | 3.3V | 100k PD | LVDS panel power enable | 945GME |
| LVDS_BKLT_EN | O | CMOS | 3.3V | 3.3V | 100k PD | LVDS panel backlight enable | 945GME |
| LVDS_BKLT_CTL | O | CMOS | 3.3V | 3.3V | 100k PD | LVDS panel backlight brightness control | 945GME |
| LVDS_I2C_CK | O | CMOS | 3.3V | 3.3V | 10k PU | I2C clock output for LVDS display use | 945GME |
| LVDS_I2C_DAT | I/O OD | CMOS | 3.3V | 3.3V | 10k PU | I2C data line for LVDS display use | 945GME |

2.9.11 LPC Bus

| Signal | Pin Type | Signal Level | Power Rail | Remark / Power Tol. | PU/PD | Description | Source / Target |
|---------------|----------|--------------|------------|---------------------|--------|---|-----------------|
| LPC_AD[0:3] | I/O | CMOS | 3.3V | 3.3V | | LPC multiplexed address, command and data bus | ICH7-M/DH |
| LPC_FRAME# | O | CMOS | 3.3V | 3.3V | | LPC frame indicates the start of an LPC cycle | ICH7-M/DH |
| LPC_DRQ[0:1]# | I | CMOS | 3.3V | 3.3V | 10k PU | LPC serial DMA request | ICH7-M/DH |
| LPC_SERIRQ | I/O | CMOS | 3.3V | 3.3V | | LPC serial interrupt | ICH7-M/DH |
| LPC_CLK | O | CMOS | 3.3V | 3.3V | | LPC clock output - 33MHz nominal | ICH7-M/DH |

2.9.12 Analog VGA

| Signal | Pin Type | Signal Level | Power Rail | Remark / Power Tol. | PU/PD | Description | Source / Target |
|-------------|----------|--------------|------------|---------------------|---------|---|-----------------|
| VGA_RED | O | Analog | | | 150R PD | Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load. | 945GME |
| VGA_GRN | O | Analog | | | 150R PD | Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load. | 945GME |
| VGA_BLU | O | Analog | | | 150R PD | Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load. | 945GME |
| VGA_HSYNC | O | CMOS | 3.3V | 3.3V | | Horizontal sync output to VGA monitor | 945GME |
| VGA_VSYNC | O | CMOS | 3.3V | 3.3V | | Vertical sync output to VGA monitor | 945GME |
| VGA_I2C_CK | O | CMOS | 3.3V | 3.3V | 2k2 PU | DDC clock line (I2C port dedicated to identify VGA monitor capabilities) | 945GME |
| VGA_I2C_DAT | I/O OD | CMOS | 3.3V | 3.3V | 2k2 PU | DDC data line. | 945GME |

2.9.13 TV Out

| Signal | Pin Type | Signal Level | Power Rail | Remark / Power Tol. | PU/PD | Description | Source / Target |
|----------|----------|--------------|------------|---------------------|-------|--|-----------------|
| TV_DAC_A | O | Analog | | | | TVDAC Channel A Output supports the following: Composite video: not used CVBS Component video: Chrominance (Pb) analog signal S-Video: not used | Not supported |
| TV_DAC_B | O | Analog | | | | TVDAC Channel B Output supports the following: Composite video: not used Component video: Luminance (Y) analog signal S-Video: Luminance analog signal. | Not supported |
| TV_DAC_C | O | Analog | | | | TVDAC Channel C Output supports the following: Composite video: not used Component: Chrominance (Pr) analog signal. S-Video: Chrominance analog signal. | Not supported |

2.9.14 SDVO

| Signal | Pin Type | Signal Level | Power Rail | Remark / Power Tol. | PU/PD | Description | Source / Target |
|----------------------------------|----------|--------------|------------|-----------------------|-------|---|-----------------|
| SDVOB_RED+ SDVOB_RED- | O | PCle | | AC coupled on module | | Serial Digital Video B red output differential pair Multiplexed with PEG_TX[0]+ and PEG_TX[0]- pair | 945GME |
| SDVOB_GRN+ SDVOB_GRN- | O | PCle | | AC coupled on module | | Serial Digital Video B green output differential pair Multiplexed with PEG_TX[1]+ and PEG_TX[1]- | 945GME |
| SDVOB_BLU+ SDVOB_BLU- | O | PCle | | AC coupled on module | | Serial Digital Video B blue output differential pair Multiplexed with PEG_TX[2]+ and PEG_TX[2]- | 945GME |
| SDVOB_CK+ SDVOB_CK- | O | PCle | | AC coupled on module | | Serial Digital Video B clock output differential pair. Multiplexed with PEG_TX[3]+ and PEG_TX[3]- | 945GME |
| SDVOB_INT+ SDVOB_INT- | I | PCle | | AC coupled off module | | Serial Digital Video B interrupt input differential pair. Multiplexed with PEG_RX[1]+ and PEG_RX[1]- | 945GME |
| SDVOC_RED+ SDVOC_RED- | O | PCle | | AC coupled on module | | Serial Digital Video C red output differential pair. Multiplexed with PEG_TX[4]+ and PEG_TX[4]- | 945GME |
| SDVOC_GRN+ SDVOC_GRN- | O | PCle | | AC coupled on module | | Serial Digital Video C green output differential pair. Multiplexed with PEG_TX[5]+ and PEG_TX[5]- | 945GME |
| SDVOC_BLU+ SDVOC_BLU- | O | PCle | | AC coupled on module | | Serial Digital Video C blue output differential pair. Multiplexed with PEG_TX[6]+ and PEG_TX[6]- | 945GME |
| SDVOC_CK+ SDVOC_CK- | O | PCle | | AC coupled on module | | Serial Digital Video C clock output differential pair. Multiplexed with PEG_TX[7]+ and PEG_TX[7]- | 945GME |
| SDVOC_INT+ SDVOC_INT- | I | PCle | | AC coupled off module | | Serial Digital Video C interrupt input differential pair. Multiplexed with PEG_RX[5]+ and PEG_RX[5]- | 945GME |
| SDVO_TVCLKIN+ SDVO_TVCLKIN- | I | PCle | | AC coupled off module | | Serial Digital Video TVOUT synchronization clock input differential pair. Multiplexed with PEG_RX[0]+ and PEG_RX[0]- | Not supported |
| SDVO_FLDSTALL+ SDVO_FLDSTALL- | I | PCle | | AC coupled off | | Serial Digital Video Field Stall input differential pair. Multiplexed with PEG_RX[2]+ and PEG_RX[2]- | 945GME |

| Signal | Pin Type | Signal Level | Power Rail | Remark / Power Tol. | PU/PD | Description | Source / Target |
|--------------|-----------|--------------|------------|---------------------|-------|---|-----------------|
| | | | | module | | | |
| SDVO_I2C_CK | O | CMOS | 2.5V | 2.5V | | SDVO I2C clock line - to set up SDVO peripherals. | 945GME |
| SDVO_I2C_DAT | I/O OD | CMOS | 2.5V | 2.5V | | SDVO I2C data line - to set up SDVO peripherals. | 945GME |

2.9.15 Miscellaneous

| Signal | Pin Type | Signal Level | Power Rail | Remark / Power Tol. | PU/PD | Description | Source / Target |
|---------------|----------|--------------|------------|---------------------|--------|---|-------------------|
| I2C_CK | O | CMOS | 3.3V | 3.3V | 2k2 PU | General purpose I2C port clock output | ICH7-M/DH / GPIO2 |
| I2C_DAT | I/O | CMOS | 3.3V | 3.3V | 2k2 PU | General purpose I2C port data I/O line | ICH7-M/DH / GPIO1 |
| SPKR | O | CMOS | 3.3V | 3.3V | 20k PD | Output for audio enunciator - the "speaker" in PC-AT systems | ICH7M-DH |
| BIOS_DISABLE# | I | CMOS | 3.3V | 3.3V | 10k PU | Module BIOS disable input. Pull low to disable on-module BIOS and use external an BIOS on the carrier board instead. | FWH |
| WDT | O | CMOS | 3.3V | 3.3V | | Output indicating that a watchdog time-out event has occurred. | PIC12F509 |
| KBD_RST# | I | CMOS | 3.3V | 3.3V | 10k PU | Input to module from (optional) external keyboard controller that can force a reset. Pulled high on the module. This is a legacy artifact of the PC-AT. | ICH7-M/DH |
| KBD_A20GATE | I | CMOS | 3.3V | 3.3V | 10k PU | Input to module from (optional) external keyboard controller that can be used to control the CPU A20 gate line. The A20GATE restricts the memory access to the bottom megabyte and is a legacy artifact of the PC- AT. Pulled high on the module. | ICH7-M/DH |

2.9.16 Power and System Management

| Signal | Pin Type | Signal Level | Power Rail | Remark / Power Tol. | PU/PD | Description | Source / Target |
|------------|----------|--------------|------------|---------------------|--------|--|-----------------|
| PWRBTN# | I | CMOS | 3.3V Sus. | 3.3V | 20k PU | Power button to bring system out of Suspend states, active on falling edge. | ICH7-M/DH |
| SYS_RESET# | I | CMOS | 3.3V Sus. | 3.3V | | Reset button input. The SYS_RESET# signal is connected directly to the chipset which reacts only to a short pulse on that line. The pulse must be least 16ms long. Pulling the signal permanently low will not hold the board in reset. | ICH7-M/DH |

| Signal | Pin Type | Signal Level | Power Rail | Remark / Power Tol. | PU/PD | Description | Source / Target |
|------------|-----------|--------------|------------|---------------------|------------|---|------------------------------|
| CB_RESET# | O | CMOS | 3.3V Sus. | 3.3V | | Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software. | ICH7-M/DH |
| PWR_OK | I | CMOS | 3.3V Sus. | 3.3V | 220k PU | Power OK from main power supply. A high value indicates that the power is good. | Power Good logic |
| SUS_STAT# | O | CMOS | 3.3V Sus. | 3.3V | | Indicates imminent suspend operation; used to notify LPC devices. | ICH7-M/DH |
| SUS_S3# | O | CMOS | 3.3V Sus. | 3.3V | | Indicates system is in Suspend to RAM state. Active low output. | ICH7-M/DH |
| SUS_S4# | O | CMOS | 3.3V Sus. | 3.3V | | Indicates system is in Suspend to Disk state. Active low output. | ICH7-M/DH |
| SUS_S5# | O | CMOS | 3.3V Sus. | 3.3V | | Indicates system is in Soft Off state. Also known as "PS_ON" and can be used to control an ATX power supply. | ICH7-M/DH |
| WAKE0# | I | CMOS | 3.3V Sus. | 3.3V | 1k PU | PCI Express wake up signal. | ICH7-M/DH |
| WAKE1# | I | CMOS | 3.3V Sus. | 3.3V | 10k PU | General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity. | ICH7M-DH GPIO13 |
| BATLOW# | I | CMOS | 3.3V Sus. | 3.3V | 220k PU | Indicates that external battery is low. | ICH7-M/DH |
| THRM# | I | CMOS | 3.3V | 3.3V | | Input from off-module temp sensor indicating an over-temp situation. | ICH7-M/DH |
| THERMTRIP# | O | CMOS | 3.3V | 3.3V | 330R PU | Active low output indicating that the CPU has entered thermal shutdown. | CPU, 945GME, ICH7-M/DH |
| SMB_CK | I/O OD | CMOS | 3.3V Sus. | 3.3V | Act. PU | System Management Bus bidirectional clock line. Power sourced through 5V standby rail and main power rails. | ICH7-M/DH |
| SMB_DAT | I/O OD | CMOS | 3.3V Sus. | 3.3V | Act. PU | System Management Bus bidirectional data line. Power sourced through 5V standby rail and main power rails. | ICH7-M/DH |
| SMB_ALERT# | I | CMOS | 3.3V Sus. | 3.3V | 10k PU | System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 5V standby rail and main power rails. | ICH7-M/DH |

2.9.17 General Purpose I/O

| Signal | Pin Type | Signal Level | Power Rail | Remark / Power Tol. | PU/PD | Description | Source / Target |
|-----------|----------|--------------|------------|---------------------|--------|---|-----------------------------|
| GPO[0..1] | O | CMOS | 3.3V | 3.3V | | General purpose output pins. | ICH7-M/DH GPIO[33, 34] |
| GPO[2..3] | O | CMOS | 3.3V | 3.3V | 8k2 PD | Upon a hardware reset, these outputs are low. | ICH7-M/DH GPIO[38, 39] |
| GPI[0:3] | I | CMOS | 3.3V | 3.3V | 10k PU | General purpose input pins. | ICH7-M/DH GPIO[21,19,36,37] |

2.9.18 Module Type Definition

| Signal | Pin Type | Signal Level | Power Rail | Remark / Power Tol. | PU/PD | Description | Source / Target | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|-------------|--------------|---------------------------------|---------------------|-------|---|-----------------|--------|--------|--|---|---|---|----------------|----|----|----|----------------|----|----|-----|-------------------------|----|-----|----|-------------------------|----|-----|-----|---------------------------------|--|
| TYPE[0:2]# | Type Detect | | | | | <p>The TYPE pins indicate to the Carrier Board the Pin-out type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pin-out Type 1, these pins are don't care (X).</p> <table border="0"> <tr> <td>TYPE2#</td> <td>TYPE1#</td> <td>TYPE0#</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>X</td> <td>Pin-out Type 1</td> </tr> <tr> <td>NC</td> <td>NC</td> <td>NC</td> <td>Pin-out Type 2</td> </tr> <tr> <td>NC</td> <td>NC</td> <td>GND</td> <td>Pin-out Type 3 (no IDE)</td> </tr> <tr> <td>NC</td> <td>GND</td> <td>NC</td> <td>Pin-out Type 4 (no PCI)</td> </tr> <tr> <td>NC</td> <td>GND</td> <td>GND</td> <td>Pin-out Type 5 (no IDE, no PCI)</td> </tr> </table> <p>The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin- out type is detected. The Carrier Board logic may also implement a fault indicator such as a LED.</p> | TYPE2# | TYPE1# | TYPE0# | | X | X | X | Pin-out Type 1 | NC | NC | NC | Pin-out Type 2 | NC | NC | GND | Pin-out Type 3 (no IDE) | NC | GND | NC | Pin-out Type 4 (no PCI) | NC | GND | GND | Pin-out Type 5 (no IDE, no PCI) | For this Type 2 board, all Type Detect pins are n.c. |
| TYPE2# | TYPE1# | TYPE0# | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | X | X | Pin-out Type 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| NC | NC | NC | Pin-out Type 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| NC | NC | GND | Pin-out Type 3 (no IDE) | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| NC | GND | NC | Pin-out Type 4 (no PCI) | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| NC | GND | GND | Pin-out Type 5 (no IDE, no PCI) | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

2.9.19 Power and GND

| Signal | Pin Type | Signal Level | Power Rail | Remark / Power Tol. | PU/PD | Description | Source / Target |
|------------|----------|--------------|------------|---------------------|-------|--|-----------------------|
| VCC_12V | Power | | 12V (±5%) | | | Primary power input: +12V (±5%) | Voltage Regulators |
| VCC_5V_SBY | Power | | 5V (±5%) | | | Standby power input: +5.0V (±5%) If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design. | VCC3.3V SUS regulator |
| VCC_RTC | Power | | | | | Real-time clock circuit-power input : +3.0V (+2.0V to +3.3V) | ICH7M-DH |
| GND | Power | | | | | Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane. | |

2.10 Pin List for MSC CXB-A945M module (Type 2)

| Row A | | Row B | | Row C | | Row D | |
|-------|----------------|-------|--------------------|-------|-------------|-------|---------------------|
| A1 | GND (FIXED) | B1 | GND (FIXED) | C1 | GND (FIXED) | D1 | GND (FIXED) |
| A2 | GBE0_MDI3- | B2 | GBE0_ACT# | C2 | IDE_D7 | D2 | IDE_D5 |
| A3 | GBE0_MDI3+ | B3 | LPC_FRAME# | C3 | IDE_D6 | D3 | IDE_D10 |
| A4 | GBE0_LINK100# | B4 | LPC_AD0 | C4 | IDE_D3 | D4 | IDE_D11 |
| A5 | GBE0_LINK1000# | B5 | LPC_AD1 | C5 | IDE_D15 | D5 | IDE_D12 |
| A6 | GBE0_MDI2- | B6 | LPC_AD2 | C6 | IDE_D8 | D6 | IDE_D4 |
| A7 | GBE0_MDI2+ | B7 | LPC_AD3 | C7 | IDE_D9 | D7 | IDE_D0 |
| A8 | GBE0_LINK# | B8 | LPC_DRQ0# | C8 | IDE_D2 | D8 | IDE_REQ |
| A9 | GBE0_MDI1- | B9 | LPC_DRQ1# | C9 | IDE_D13 | D9 | IDE_IOW# |
| A10 | GBE0_MDI1+ | B10 | LPC_CLK | C10 | IDE_D1 | D10 | IDE_ACK# |
| A11 | GND (FIXED) | B11 | GND (FIXED) | C11 | GND (FIXED) | D11 | GND (FIXED) |
| A12 | GBE0_MDI0- | B12 | PWRBTN# | C12 | IDE_D14 | D12 | IDE_IRQ |
| A13 | GBE0_MDI0+ | B13 | SMB_CK | C13 | IDE_IORDY | D13 | IDE_A0 |
| A14 | GBE0_CTREF | B14 | SMB_DAT | C14 | IDE_IOR# | D14 | IDE_A1 |
| A15 | SUS_S3# | B15 | SMB_ALERT# | C15 | PCI_PME# | D15 | IDE_A2 |
| A16 | SATA0_TX+ | B16 | SATA1_TX+ | C16 | PCI_GNT2# | D16 | IDE_CS1# |
| A17 | SATA0_TX- | B17 | SATA1_TX- | C17 | PCI_REQ2# | D17 | IDE_CS3# |
| A18 | SUS_S4# | B18 | SUS_STAT# | C18 | PCI_GNT1# | D18 | IDE_RESET# |
| A19 | SATA0_RX+ | B19 | SATA1_RX+ | C19 | PCI_REQ1# | D19 | PCI_GNT3# |
| A20 | SATA0_RX- | B20 | SATA1_RX- | C20 | PCI_GNT0# | D20 | PCI_REQ3# |
| A21 | GND (FIXED) | B21 | GND (FIXED) | C21 | GND (FIXED) | D21 | GND (FIXED) |
| A22 | SATA2_TX+ | B22 | SATA3_TX+ | C22 | PCI_REQ0# | D22 | PCI_AD1 |
| A23 | SATA2_TX- | B23 | SATA3_TX- | C23 | PCI_RESET# | D23 | PCI_AD3 |
| A24 | SUS_S5# | B24 | PWR_OK | C24 | PCI_AD0 | D24 | PCI_AD5 |
| A25 | SATA2_RX+ | B25 | SATA3_RX+ | C25 | PCI_AD2 | D25 | PCI_AD7 |
| A26 | SATA2_RX- | B26 | SATA3_RX- | C26 | PCI_AD4 | D26 | PCI_C/BE0# |
| A27 | BATLOW# | B27 | WDT | C27 | PCI_AD6 | D27 | PCI_AD9 |
| A28 | ATA_ACT# | B28 | AC_SDIN2 | C28 | PCI_AD8 | D28 | PCI_AD11 |
| A29 | AC_SYNC | B29 | AC_SDIN1 | C29 | PCI_AD10 | D29 | PCI_AD13 |
| A30 | AC_RST# | B30 | AC_SDIN0 | C30 | PCI_AD12 | D30 | PCI_AD15 |
| A31 | GND (FIXED) | B31 | GND (FIXED) | C31 | GND (FIXED) | D31 | GND (FIXED) |
| A32 | AC_BITCLK | B32 | SPKR | C32 | PCI_AD14 | D32 | PCI_PAR |
| A33 | AC_SDOUT | B33 | I2C_CK | C33 | PCI_C/BE1# | D33 | PCI_SERR# |
| A34 | BIOS_DISABLE# | B34 | I2C_DAT | C34 | PCI_PERR# | D34 | PCI_STOP# |
| A35 | THRMTRIP# | B35 | THRM# | C35 | PCI_LOCK# | D35 | PCI_TRDY# |
| A36 | USB6- | B36 | USB7- | C36 | PCI_DEVSEL# | D36 | PCI_FRAME# |
| A37 | USB6+ | B37 | USB7+ | C37 | PCI_IRDY# | D37 | PCI_AD16 |
| A38 | USB_6_7_OC# | B38 | USB_4_5_OC# | C38 | PCI_C/BE2# | D38 | PCI_AD18 |
| A39 | USB4- | B39 | USB5- | C39 | PCI_AD17 | D39 | PCI_AD20 |
| A40 | USB4+ | B40 | USB5+ | C40 | PCI_AD19 | D40 | PCI_AD22 |
| A41 | GND (FIXED) | B41 | GND (FIXED) | C41 | GND (FIXED) | D41 | GND (FIXED) |
| A42 | USB2- | B42 | USB3- | C42 | PCI_AD21 | D42 | PCI_AD24 |
| A43 | USB2+ | B43 | USB3+ | C43 | PCI_AD23 | D43 | PCI_AD26 |
| A44 | USB_2_3_OC# | B44 | USB_0_1_OC# | C44 | PCI_C/BE3# | D44 | PCI_AD28 |
| A45 | USB0- | B45 | USB1- | C45 | PCI_AD25 | D45 | PCI_AD30 |
| A46 | USB0+ | B46 | USB1+ | C46 | PCI_AD27 | D46 | PCI_IRQC# |
| A47 | VCC_RTC | B47 | EXCD1_PERST# | C47 | PCI_AD29 | D47 | PCI_IRQD# |
| A48 | EXCD0_PERST# | B48 | n.c. (EXCD1_CPPE#) | C48 | PCI_AD31 | D48 | PCI_CLKRUN# |
| A49 | EXCD0_CPPE# | B49 | SYS_RESET# | C49 | PCI_IRQA# | D49 | n.c. (PCI_M66EN) |
| A50 | LPC_SERIRQ | B50 | CB_RESET# | C50 | PCI_IRQB# | D50 | PCI_CLK |

| | |
|--|---|
| | = not supported on MSC CXB-A945M module |
|--|---|

| Row A | | Row B | | Row C | | Row D | |
|-------|------------------|-------|------------------|-------|-------------|-------|--------------|
| A51 | GND (FIXED) | B51 | GND (FIXED) | C51 | GND (FIXED) | D51 | GND (FIXED) |
| A52 | n.c. (PCIE_TX5+) | B52 | n.c. (PCIE_RX5+) | C52 | PEG_RX0+ | D52 | PEG_TX0+ |
| A53 | n.c. (PCIE_TX5-) | B53 | n.c. (PCIE_RX5-) | C53 | PEG_RX0- | D53 | PEG_TX0- |
| A54 | GPI0 | B54 | GPO1 | C54 | TYPE0# | D54 | PEG_LANE_RV# |
| A55 | PCIE_TX4+ | B55 | PCIE_RX4+ | C55 | PEG_RX1+ | D55 | PEG_TX1+ |
| A56 | PCIE_TX4- | B56 | PCIE_RX4- | C56 | PEG_RX1- | D56 | PEG_TX1- |
| A57 | GND | B57 | GPO2 | C57 | TYPE1# | D57 | TYPE2# |
| A58 | PCIE_TX3+ | B58 | PCIE_RX3+ | C58 | PEG_RX2+ | D58 | PEG_TX2+ |
| A59 | PCIE_TX3- | B59 | PCIE_RX3- | C59 | PEG_RX2- | D59 | PEG_TX2- |
| A60 | GND (FIXED) | B60 | GND (FIXED) | C60 | GND (FIXED) | D60 | GND (FIXED) |
| A61 | PCIE_TX2+ | B61 | PCIE_RX2+ | C61 | PEG_RX3+ | D61 | PEG_TX3+ |
| A62 | PCIE_TX2- | B62 | PCIE_RX2- | C62 | PEG_RX3- | D62 | PEG_TX3- |
| A63 | GPI1 | B63 | GPO3 | C63 | RSVD | D63 | RSVD |
| A64 | PCIE_TX1+ | B64 | PCIE_RX1+ | C64 | RSVD | D64 | RSVD |
| A65 | PCIE_TX1- | B65 | PCIE_RX1- | C65 | PEG_RX4+ | D65 | PEG_TX4+ |
| A66 | GND | B66 | WAKE0# | C66 | PEG_RX4- | D66 | PEG_TX4- |
| A67 | GPI2 | B67 | WAKE1# | C67 | RSVD | D67 | GND |
| A68 | PCIE_TX0+ | B68 | PCIE_RX0+ | C68 | PEG_RX5+ | D68 | PEG_TX5+ |
| A69 | PCIE_TX0- | B69 | PCIE_RX0- | C69 | PEG_RX5- | D69 | PEG_TX5- |
| A70 | GND (FIXED) | B70 | GND (FIXED) | C70 | GND (FIXED) | D70 | GND (FIXED) |
| A71 | LVDS_A0+ | B71 | LVDS_B0+ | C71 | PEG_RX6+ | D71 | PEG_TX6+ |
| A72 | LVDS_A0- | B72 | LVDS_B0- | C72 | PEG_RX6- | D72 | PEG_TX6- |
| A73 | LVDS_A1+ | B73 | LVDS_B1+ | C73 | SDVO_DATA | D73 | SDVO_CLK |
| A74 | LVDS_A1- | B74 | LVDS_B1- | C74 | PEG_RX7+ | D74 | PEG_TX7+ |
| A75 | LVDS_A2+ | B75 | LVDS_B2+ | C75 | PEG_RX7- | D75 | PEG_TX7- |
| A76 | LVDS_A2- | B76 | LVDS_B2- | C76 | GND | D76 | GND |
| A77 | LVDS_VDD_EN | B77 | LVDS_B3+ | C77 | RSVD | D77 | IDE_CBLID# |
| A78 | LVDS_A3+ | B78 | LVDS_B3- | C78 | PEG_RX8+ | D78 | PEG_TX8+ |
| A79 | LVDS_A3- | B79 | LVDS_BKLT_EN | C79 | PEG_RX8- | D79 | PEG_TX8- |
| A80 | GND (FIXED) | B80 | GND (FIXED) | C80 | GND (FIXED) | D80 | GND (FIXED) |
| A81 | LVDS_A_CK+ | B81 | LVDS_B_CK+ | C81 | PEG_RX9+ | D81 | PEG_TX9+ |
| A82 | LVDS_A_CK- | B82 | LVDS_B_CK- | C82 | PEG_RX9- | D82 | PEG_TX9- |
| A83 | LVDS_I2C_CK | B83 | LVDS_BKLT_CTRL | C83 | RSVD | D83 | RSVD |
| A84 | LVDS_I2C_DAT | B84 | VCC_5V_SBY | C84 | GND | D84 | GND |
| A85 | GPI3 | B85 | VCC_5V_SBY | C85 | PEG_RX10+ | D85 | PEG_TX10+ |
| A86 | KBD_RST# | B86 | VCC_5V_SBY | C86 | PEG_RX10- | D86 | PEG_TX10- |
| A87 | KBD_A20GATE | B87 | VCC_5V_SBY | C87 | GND | D87 | GND |
| A88 | PCIE0_CK_REF+ | B88 | RSVD | C88 | PEG_RX11+ | D88 | PEG_TX11+ |
| A89 | PCIE0_CK_REF- | B89 | VGA_RED | C89 | PEG_RX11- | D89 | PEG_TX11- |
| A90 | GND (FIXED) | B90 | GND (FIXED) | C90 | GND (FIXED) | D90 | GND (FIXED) |
| A91 | RSVD | B91 | VGA_GRN | C91 | PEG_RX12+ | D91 | PEG_TX12+ |
| A92 | RSVD | B92 | VGA_BLU | C92 | PEG_RX12- | D92 | PEG_TX12- |
| A93 | GPO0 | B93 | VGA_HSYNC | C93 | GND | D93 | GND |
| A94 | RSVD | B94 | VGA_VSYNC | C94 | PEG_RX13+ | D94 | PEG_TX13+ |
| A95 | RSVD | B95 | VGA_I2C_CK | C95 | PEG_RX13- | D95 | PEG_TX13- |
| A96 | GND | B96 | VGA_I2C_DAT | C96 | GND | D96 | GND |
| A97 | VCC_12V | B97 | n.c. (TV_DAC_A) | C97 | RSVD | D97 | PEG_ENABLE# |
| A98 | VCC_12V | B98 | n.c. (TV_DAC_B) | C98 | PEG_RX14+ | D98 | PEG_TX14+ |
| A99 | VCC_12V | B99 | n.c. (TV_DAC_C) | C99 | PEG_RX14- | D99 | PEG_TX14- |
| A100 | GND (FIXED) | B100 | GND (FIXED) | C100 | GND (FIXED) | D100 | GND (FIXED) |
| A101 | VCC_12V | B101 | VCC_12V | C101 | PEG_RX15+ | D101 | PEG_TX15+ |
| A102 | VCC_12V | B102 | VCC_12V | C102 | PEG_RX15- | D102 | PEG_TX15- |
| A103 | VCC_12V | B103 | VCC_12V | C103 | GND | D103 | GND |
| A104 | VCC_12V | B104 | VCC_12V | C104 | VCC_12V | D104 | VCC_12V |
| A105 | VCC_12V | B105 | VCC_12V | C105 | VCC_12V | D105 | VCC_12V |
| A106 | VCC_12V | B106 | VCC_12V | C106 | VCC_12V | D106 | VCC_12V |

| | | | | | | | |
|------|-------------|------|-------------|------|-------------|------|-------------|
| A107 | VCC_12V | B107 | VCC_12V | C107 | VCC_12V | D107 | VCC_12V |
| A108 | VCC_12V | B108 | VCC_12V | C108 | VCC_12V | D108 | VCC_12V |
| A109 | VCC_12V | B109 | VCC_12V | C109 | VCC_12V | D109 | VCC_12V |
| A110 | GND (FIXED) | B110 | GND (FIXED) | C110 | GND (FIXED) | D110 | GND (FIXED) |

| | |
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| | = not supported on MSC CXB-A945M module |
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2.11 Watchdog

The module has a watchdog function implemented using a PIC microcontroller with an SM-Bus interface. The watchdog can be enabled and configured in the BIOS SETUP.

If the watchdog is enabled a counter is started which generates a reset if it is not retriggered within a programmable time window.

The watchdog menu in the BIOS provides the following parameters:

Watchdog: Enabled / **Disabled** (default)

Initial Delay: 1s, 5s, 10s, **30s** (default), 1min, 5min, 10min, 30min

Timeout: 0.4s, 1s, 5s, 10s, **30s** (default), 1min, 5 min, 10min

Start on Boot: if yes, watchdog starts at the end of POST (power on self test) before the OS is loaded

| ICH7M Pin | Label | Description |
|-----------|--------|---|
| GPIO6 | WDEN | Watchdog Enable. 1 = watchdog counter counts |
| GPIO35 | WDTRIG | Watchdog Trigger. If watchdog is enabled (WDEN=1), the signal level on this line has to be inverted within the timeout delay to trigger this chip (which means to avoid to get a reset) |
| GPIO7 | WDSTS | Watchdog Status. 0 = no Timeout , Default after Power-Up or after setting of Bit0. 1 = Timeout event has occurred; a reset has been triggered. In this case, the watchdog counter will be stopped. |

Programming information, register layout etc. can be found in the ICH7M-DH datasheet.

The timeout and the delay time can be written into the watchdog controller via the SMB. The register layout is as follows:

| Address | Data Byte | Default value | Read/Write | Bit | Remark |
|---------|-------------------|---------------|------------|------|--------|
| 0 | TimeOut low Byte | 100d | W | Byte | |
| 1 | TimeOut high Byte | 0 | W | Byte | |
| 2 | Delay low Byte | 100d | W | Byte | |
| 3 | Delay high Byte | 0 | W | Byte | |

The SMB-Address of the watchdog controller is B0h/B1h. The data structure to access the byte registers is:

Device Address B0 - Register Address - Data Byte

Reading of these registers is not supported. While writing into these registers, the watchdog timer has to be stopped. For information about accessing the SMB please refer to the Intel® ICH7M-DH datasheet.

3 System resources

3.1 PCI Devices MSC CXB-A945M

| Slot Number (or Onboard Device) | IDSEL # or DEV. # | Bus # | Interrupts of Controller (ICH-7M) | | | | | | | |
|---------------------------------------|-------------------------|-------|-----------------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| | | | PIRQ 0 (INT A) | PIRQ 1 (INT B) | PIRQ 2 (INT C) | PIRQ 3 (INT D) | PIRQ 4 (INT E) | PIRQ 5 (INT F) | PIRQ 6 (INT G) | PIRQ 7 (INT H) |
| 1 | AD20 / Dev 04h | - | A | B | C | D | | | | |
| 2 | AD21 / Dev 05h | - | D | A | B | C | | | | |
| 3 | AD22 / Dev 06h | - | C | D | A | B | | | | |
| 4 | AD23 / Dev 07h | - | B | C | D | A | | | | |
| Internal Graphic Device | Dev 02h | 0 | A | -- | - | -- | | | | |
| PCI Express Root Port | Dev 28 Fkt 0/1/2/3 | 0 | A | B | C | D | | | | |
| USB UHCI Host Controller | Dev 29 Fkt 0 | 0 | | | | | A | | | |
| USB UHCI Host Controller | Dev 29 Fkt 1 | 0 | | | | | | B | | |
| USB UHCI Host Controller | Dev 29 Fkt 2 | 0 | | | | | | | C | |
| USB UHCI Host Controller | Dev 29 Fkt 3 | 0 | | | | | | | | D |
| USB EHCI Controller | Dev 29 Fkt 7 | 0 | | | | | | | | D |
| AC '97 Audio | Dev 30 Fkt 2 | 0 | | | | | | | A | |
| SATA | Dev 31 Fkt 2 | 0 | | | | | | B | | |
| PATA | Dev 31 Fkt 1 | 0 | | | | | | B | | |
| SMBus | Dev 31 Fkt 3 | 0 | | | | | | B | | |
| 100MB Lan Controller | Dev 8 Fkt 0 | - | | | | | A | | | |
| PCIe Slot 1 | Dev 0 Fkt 0 | - | A | B | C | D | | | | |
| PCIe Slot 2 | Dev 0 Fkt 0 | - | D | A | B | C | | | | |
| PCIe Slot 3 | Dev 0 Fkt 0 | - | C | D | A | B | | | | |
| PCIe Slot 4 | Dev 0 Fkt 0 | - | B | C | D | A | | | | |
| PCIe Slot 5 | Dev 0 fkt 0 | - | A | B | C | D | | | | |

| | | | Interrupts of Controller (ICH-7M) | | | | | | | |
|---|-------------------------|-------|-----------------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Slot Number (or Onboard Device) | IDSEL # or DEV. # | Bus # | PIRQ 0 (INT A) | PIRQ 1 (INT B) | PIRQ 2 (INT C) | PIRQ 3 (INT D) | PIRQ 4 (INT E) | PIRQ 5 (INT F) | PIRQ 6 (INT G) | PIRQ 7 (INT H) |
| PCIe Slot 6 Or GB Lan Controller | | | D | A | B | C | | | | |

3.2 Carrier Board PCI Resource Allocation

The external PCI resource allocation on the carrier board should be as follows:

| Slot / Device Signal | Slot / Device 0 | Slot / Device 1 | Slot / Device 2 | Slot / Device 3 |
|----------------------|-----------------|-----------------|-----------------|-----------------|
| IDSEL | PCI_AD[20] | PCI_AD[21] | PCI_AD[22] | PCI_AD[23] |
| PCI Clock | PCI_CLK replica | PCI_CLK replica | PCI_CLK replica | PCI_CLK replica |
| INTA# | PCI_IRQ[A]# | PCI_IRQ[B]# | PCI_IRQ[C]# | PCI_IRQ[D]# |
| INTB# (if used) | PCI_IRQ[B]# | PCI_IRQ[C]# | PCI_IRQ[D]# | PCI_IRQ[A]# |
| INTC# (if used) | PCI_IRQ[C]# | PCI_IRQ[D]# | PCI_IRQ[A]# | PCI_IRQ[B]# |
| INTD# (if used) | PCI_IRQ[D]# | PCI_IRQ[A]# | PCI_IRQ[B]# | PCI_IRQ[C]# |
| REQ0# (if used) | PCI_REQ[0]# | PCI_REQ[1]# | PCI_REQ[2]# | PCI_REQ[3]# |
| REQ1# (if used) | PCI_REQ[1]# | PCI_REQ[2]# | PCI_REQ[3]# | PCI_REQ[0]# |
| REQ2# (if used) | PCI_REQ[2]# | PCI_REQ[3]# | PCI_REQ[0]# | PCI_REQ[1]# |
| REQ3# (if used) | PCI_REQ[3]# | PCI_REQ[0]# | PCI_REQ[1]# | PCI_REQ[2]# |
| GNT0# (if used) | PCI_GNT[0]# | PCI_GNT[1]# | PCI_GNT[2]# | PCI_GNT[3]# |
| GNT1# (if used) | PCI_GNT[1]# | PCI_GNT[2]# | PCI_GNT[3]# | PCI_GNT[0]# |
| GNT2# (if used) | PCI_GNT[2]# | PCI_GNT[3]# | PCI_GNT[0]# | PCI_GNT[1]# |
| GNT3# (if used) | PCI_GNT[3]# | PCI_GNT[0]# | PCI_GNT[1]# | PCI_GNT[2]# |

The signals PCI_IRQx, PCI_REQx or PCI_GNTx are routed exclusively to the COM Express connector. They are not shared on the CPU board.

3.3 SMB Address Map

| Device | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | Address ¹⁾ |
|----------------------------------|----|----|----|----|----|----|----|-----|-----------------------|
| SMBus host (ICH7-M/DH slave) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | x | 10h / 08h |
| GigaBit LAN | | | | | | | | | |
| Winbond W83L786R ²⁾ | 0 | 1 | 0 | 1 | 1 | 1 | 0 | x | 5Ch / 2Eh |
| Winbond W83L771AWG ²⁾ | 1 | 0 | 0 | 1 | 1 | 0 | 0 | x | 98h / 4Ch |
| SMCS EMC2104 ²⁾ | 0 | 1 | 0 | 1 | 1 | 1 | 1 | x | 5Eh / 2Fh |
| Watchdog (PIC12F509) | 1 | 0 | 1 | 1 | 0 | 0 | 0 | x | B0h / 58h |
| CY28411 Clock Synthesizer | 1 | 1 | 0 | 1 | 0 | 0 | 1 | x | D2h / 69h |
| CY25823 Clock Synthesizer | 1 | 1 | 0 | 1 | 0 | 1 | 0 | x | D4h / 6Ah |
| CMOS backup EEPROM | 1 | 0 | 1 | 0 | 1 | 0 | 0 | x | A8h / 54h |
| SPD EEPROM (SO-DIMM) | 1 | 0 | 1 | 0 | 0 | 0 | 0 | x | A0h / 50h |

1) 8 bit address (with R/W) / 7 bit address (without R/W)

2) System monitoring devices Winbond W83L786G and W83L771AWG on hardware revision V1.0 were replaced with SMSC device EMC2104 on revision V2.0 modules.

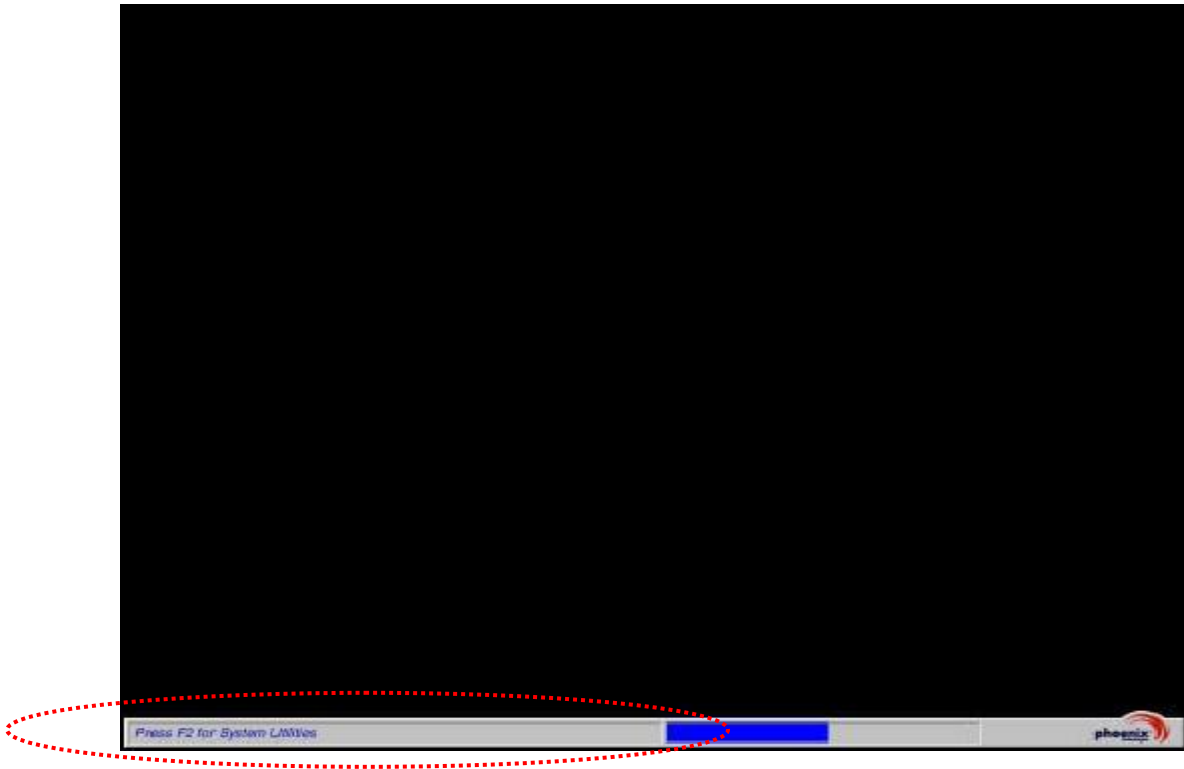
4 BIOS

4.1 Introduction

This guide describes the Phoenix TrustedCore Startup screen and contains information on how to access Phoenix TrustedCore setup to modify the settings which control Phoenix pre-OS (operating system) functions.

4.1.1 Startup Screen Overview

The Phoenix TrustedCore Startup screen is a graphical user interface (GUI) that is included in Phoenix TrustedCore products. The default bios behavior is to show an informational text screen during bios POST phase, but the graphical boot screen can be enabled in the bios setup. The standard boot screen is a black screen, including a progress bar at the bottom of the screen. This bar indicates the progress of the Startup Screen functions and provides user prompting and POST status. The following figure shows the various parts of a generic Startup Screen at 1024x768 resolution:



4.1.2 Activity Detection Background

While the TrustedCore Startup screen is displayed, press the Setup Entry key (F2 – TrustedCore default). The TrustedCore Startup Status Bar acknowledges the input, and at the end of POST, the screen clears and setup launches.

An example of the Startup Status Bar displaying changing state is shown in the following figure. The “Please Wait...” text is displayed after the F2 key is pressed to acknowledge user input.

Active status bar:



4.2 TrustedCore Setup Utility

With the Phoenix TrustedCore Setup program, you can modify TrustedCore settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning the special features on or off. This chapter provides an overview of the Setup utility and describes at a high-level how to use it.

4.2.1 Configuring the System BIOS

To start the Phoenix TrustedCore Setup utility, press [F2] to launch Setup. The Setup main menu appears.

The BIOS Menu Structure

The BIOS Menu is structured in the following way:

| | |
|-----------------|------------------------------------|
| Main | |
| | Board Information |
| | IDE Channel 0 Master |
| | IDE Channel 0 Slave |
| | SATA Port 0 |
| | SATA Port 1 |
| | Boot Options |
| Advanced | |
| | Cache Memory |
| | CPU Control Sub-Menu |
| | MCH Control Sub-menu |
| | Video (Intel IGD) Control Sub-menu |
| | ICH Control Sub-menu |
| | PCI Express Control Sub-menu |
| | PCI Control Sub-menu |
| | ICH USB Control Sub-menu |
| | ACPI Control Sub-menu |
| | Clock Control Sub-menu |
| | I/O Device Configuration |
| | Watchdog Options |
| Security | |
| Power | |
| | Hardware Monitor |
| Boot | |
| Exit | |

The Menu Bar

The Menu Bar at the top of the window lists these selections:

| Menu Items | Description |
|------------|--|
| Main | Use this menu for basic system configuration. |
| Advanced | Use this menu to set the Advanced Features available on your system's chipset. |
| Security | Use this menu to set User and Supervisor Passwords and the Backup and Virus-Check reminders. |
| Power | Use this menu to configure Power-Management features. |
| Boot | Use this menu to set the boot order in which the BIOS attempts to boot to OS. |
| Exit | Exits the current menu. |

Use the left and right arrow keys on your keyboard to make a menu selection.

The Legend Bar

Use the keys listed in the legend bar on the bottom of the screen to make your selections, or to exit the current menu. The following table describes the legend keys and their alternates:

| Key | Function |
|------------------------|---|
| F1 or Alt-H | General Help window. |
| Esc | Exit this menu. |
| Arrow keys | Select a different menu. |
| Up and down arrow keys | Move cursor up and down. |
| Tab or Shift-Tab | Move cursor left and right (i.e. at System Time / System Date). |
| Home or End | Move cursor to top or bottom of window. |
| PgUp or PgDn | Move cursor to next or previous page. |
| F5 or - | Select the previous value for the field. |
| F6 or + or Space | Select the next value for the field. |
| F9 | Load the Default Configuration values (for all menus). |
| F10 | Save and exit. |
| Enter | Execute command or select submenu. |

Select an item

To select an item, use the arrow keys to move the cursor to the field you want. Then use the plus-and-minus value keys to select a value for that field. The Save Values commands in the Exit Menu save the values currently displayed in all the menus.

Display a submenu

To display a submenu, use the arrow keys to move the cursor to the sub menu you want. Then press Enter. A pointer marks all submenus.

4.2.2 The Main Menu

You can select the following in the Main Menu. Use the sub menus for other selections.

| Feature | Options | Description |
|----------------------|---------------------------|--------------------------------|
| Board Information | Submenu | Displays BIOS Version |
| System Time | Enter Time (HH:MM:SS) | Set the System Time. |
| System Date | Enter Date (DD/MM/YYYY) | Set the System Date. |
| IDE Channel 0 Master | Submenu "Master & Slaves" | Configure IDE Channel 0 Master |
| IDE Channel 0 Slave | Submenu "Master & Slaves" | Configure IDE Channel 0 Slave |
| SATA Port 0 | Submenu "Master & Slaves" | Configure SATA Port 0 |
| SATA Port 1 | Submenu "Master & Slaves" | Configure SATA Port 1 |
| Boot Options | Submenu | Configure Boot Options |

4.2.2.1 Board Information

| Feature | Options | Description |
|-----------------|----------------|---|
| Bios Version | Informative | Shows current bios version. |
| HW Platform | Informative | Name of the hardware platform |
| HW Revision | Informative | Hardware revision number |
| Serial # | Informative | Hardware Serial Number |
| Boot Counter | Informative | The number of times this board has booted up. |
| CPU String | Informative | CPU Identification string |
| CPU Speed | Informative | CPU Speed |
| CPU Class | Informative | CPU ID Class code |
| CPU Model | Informative | CPU ID Model code |
| CPU Stepping | Informative | CPU ID Stepping |
| CPU Cores | Informative | Number of CPU cores |
| Northbridge | Informative | Identification of the northbridge |
| Southbridge | Informative | Identification of the southbridge |
| System Memory | Informative | Amount of memory below 1MB |
| Extended Memory | Informative | Total amount of memory |

4.2.2.2 Master and Slaves

The **Master** and **Slave** settings on the Main Menu control these types of devices:

- **Hard-disk drives (IDE and SATA)**
- **Removable-disk drives**
- **CD-ROM drives**

There is one IDE connector on your motherboard, usually labeled "Primary IDE". There are usually two connectors on each ribbon cable attached to IDE connector. When you have connected two drives to this connector, the one on the end of the cable is the Master.

When you enter Setup, the Main Menu displays the results of **Autotyping** information each drive provides about its own size and other characteristics—and how they are arranged as Masters or Slaves on your machine.

Note: Do not attempt to change these settings unless you have an installed drive that does not autotype properly (such as an older hard-disk drive that does not support autotyping).

If you need to change your drive settings, select one of the Master or Slave drives on the Main Menu. This will display a menu like this:

Note: The capacity is displayed in 'real' Mbytes (1MB=1024*1024 Bytes) Drives with a total capacity greater than 8Gbyte operate in LBA format only.

| Feature | Options | Description |
|------------------------|---|---|
| Type | None, ATAPI Removable, CD-ROM, IDE Removable, Other ATAPI, User, Auto | None = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed. Auto = Autotyping, the drive itself supplies the information. User = You supply the hard-disk drive information in the following fields. IDE Removable = Removable Disk Drive ATAPI Removable = Removable Disk Drive Other ATAPI = non-specific ATAPI Device CD-ROM = CD-ROM drive. |
| Cylinders | 1 to 65536 | Number of Cylinders |
| Heads | 1 to 16 | Number of read/write heads |
| Sectors | 1 to 63 | Number of sectors per track |
| Multi-Sector Transfers | Disabled, 2 sectors, 4 sectors, 8 sectors, 16 sectors | Any selection except Disabled determines the number of sectors transferred per block. |
| LBA Mode Control | Disabled, Enabled | Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, & Sectors. |

| Feature | Options | Description |
|------------------|--|---|
| 32 Bit I/O | Disabled, Enabled | Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus. |
| Transfer Mode | Standard Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO 3 / DMA 1 FPIO 4 / DMA 2 | Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform. |
| Ultra DMA Mode | Disabled Mode 0 Mode 1 Mode 2 Mode 3 Mode 4 Mode 5 | Ultra DMA Mode supports 33/66/100 MB/sec transfer rate for fixed disk drives. |
| SMART Monitoring | Disabled, Enabled | Displays the status of SMART Monitoring if supported by the used drive. |

WARNING: Incorrect settings can cause your system to malfunction.

4.2.2.3 Boot Options

| Feature | Options | Description |
|-----------------------------|----------------------------|---|
| Summary screen | Disabled, Enabled | Enabled displays system configuration on boot. |
| Boot-time Diagnostic Screen | Disabled, Enabled | Enabled displays the diagnostic screen during boot. Disabled displays the Boot Logo. |
| Post Errors | Disabled, Enabled | Pauses and displays Setup Entry or resume boot prompt if error occurs on boot. If disabled, system always attempts to boot. |
| Extended Memory Testing | Normal, Just zero it, None | Determines which type of test will be performed on extended memory during POST (above 1 MB). |

4.2.3 The Advanced Menu

| Feature | Options | Description |
|------------------------------------|---|--|
| Installed O/S | Other, Win95, Win98, WinMe, Win2000, WinXP | Select the operating system installed on your system which you will use most commonly. NOTE: An incorrect setting can cause some operating systems to display unexpected behavior. |
| Reset configuration Data | No, Yes | Select 'Yes' if you want to clear the Extended System Configuration Data (ESCD) area. |
| Large Disk Access Mode | Other, DOS | Select Other for UNIX, Novell NetWare. Select DOS for all other operating systems. |
| Small Disk Access Mode | No, Yes | Select if CHS translation should be made for a LBA-capable harddisk with less than 1024 cylinders, e.g. CompactFlash(R). If you have problems with booting from a CompactFlash(R), try to change this setting. No = translate CHS only if HDD has >1024 cyls. Yes = translate CHS for all LBA-capable disks. |
| Port 80 Cycles | LPC Bus, PCI Bus | Control where the Port 80h cycles are sent. |
| Local Bus IDE adapter | Disabled, Enabled | Enable the integrated local bus IDE adapter. |
| Cache Memory | Submenu | Configure Cache Memory |
| CPU Control Sub-Menu | Submenu | Configure CPU Control |
| MCH Control Sub-Menu | Submenu | Configure MCH Control |
| Video (Intel IGD) Control Sub-Menu | Submenu | Configure Video (Intel IGD) Control |
| ICH Control Sub-Menu | Submenu | Configure ICH Control |
| ACPI Control Sub-Menu | Submenu | Configure ACPI Control |
| Clock Control Sub-Menu | Submenu | Configure Clock Control |
| I/O Device Configuration | Submenu | Configure I/O Device |
| Watchdog Options | Submenu | Configure Watchdog Options |

4.2.3.1 Cache Memory Control Menu

| Feature | Options | Description |
|---|---|--|
| Cache System BIOS area | Uncached, Write Protect | Enables caching of system BIOS area. |
| Cache Video BIOS area | Uncached, Write Protect | Enables caching of video BIOS area. |
| Cache D000 – D3FF Cache D400 – D7FF Cache D800 – DBFF | Disabled, Write Through, Write Protect, Write Back | Disabled = This block is not cached. Write through = Writes are cached and sent to main memory at once. Write Protect = Writes are ignored. Write Back = Writes are cached but not sent to main memory until necessary. |

4.2.3.2 Atom CPU Control Sub-Menu

| Feature | Options | Description |
|----------------------------|---|--|
| Processor Power Management | Disabled, GV3 only, C-States Only, Enabled | Selects the Processor Power Management desired Disabled = C-States and GV3 are disabled. GV3 Only = C-States are disabled. C-States Only = GV3 is disabled. Enabled = C-States und GV3 are enabled. Note: GV3 refers to the speed step capability of the CPU. Note: If GV3 is disabled, OS will not run with maximum frequency. To use maximum frequency, GV3 has to be enabled and OS must Control the CPU frequency via Power managment. Note: For optimal response times the GV3 (Speed step) must be enabled and C-States disabled. |
| Enhanced C-States Enable | Disabled, Enabled | Enables Enhanced C-State support. Disabled = Enhanced C-States disabled. Enabled = Enhanced C-State enable. |

| Feature | Options | Description |
|--------------------------------|---------------------------------|--|
| Timestamp Counter Updates | Disabled, Enabled | Control TSC updates after C3/C4 through this Setup Option. |
| Thermal Control Circuit | Disabled, TM1, TM2, TM1 and TM2 | Setting this bit enables the thermal control circuit (TCC) portion of the Thermal Monitor feature of the CPU. TM1 = 50% duty Cycle TM2 = Geyserville III |
| DTS Enable | Disabled, Enabled | Enable the Atom DTS to be used for platform Thermal Management. Note: If DTS is disabled, thermal throttling in ACPI will not work. |
| No Execute Mode Mem Protection | Enabled, Disabled | |
| Set Max Ext CPUID = 3 | Disabled, Enabled | Sets Max CPUID extended function value to 3. |

4.2.3.3 MCH Control Sub-Menu

| Feature | Options | Description |
|---------------------------|-------------------|---|
| PCI Express Graphics Port | Disabled, Auto | Disabled = Port always disabled. Auto = Only enable if card found. |
| Port ASPM Support | Disabled, Auto | Control ASPM support for the PEG Device. Auto = will set APMC to the highest common supported ASPM between the Port and Endpoint. |
| GPLL Power-Down Enable: | Disabled, Enabled | Controls the ability of the PEG port to power down the GPLL. Disabled = The GPLL will always remain active. Enabled = The GPLL may be powered down. |
| MDA Support | Disabled, Enabled | Control MDA support for the PEG Device. |
| Memory Throttling | Disabled, Enabled | Controls throttling and bandwidth limiting for the GMCH. |
| Delta Temperature in SPD | Disabled, Enabled | Controls memory throttling based on thermal information present in the memory SPD. |

4.2.3.4 Video (Intel IGD) Control Sub-Menu

| Feature | Options | Description |
|-------------------------------|---|--|
| Default Primary Video Adapter | IGD, PEG | Select 'IGD' to have Internal Graphics, if supported and enabled, be used for the boot display device. Select 'PEG' to have PCI Express Graphics, if supported and enabled, be used for the boot display device. To use PCI Video, select IGD. |
| IGD – Device 2 | Disabled, Auto | Enables or Disable the Internal Graphics Device by setting item to the desired value. |
| IGD – Device 2, Function1 | Disabled, Auto | Enables or Disable Function 1 of the Internal Graphics Device by setting item to the desired value. |
| IGD – Boot Type | VBIOS default, CRT, LFP, EFP, EFP2, CRT+LFP, CRT+EFP, CRT+EFP2 | Select the Video Device that will be activated during POST. |
| IGD – LCD Panel Type | 640x480, sp, 18bit 800x600, sp, 18bit 1024x768, sp, 18bit 1280x1024, dp, 18bit 1440x900, dp, 24bit 1400x1050, dp, 24 bit 1600x1200, dp, 24 bit 1280x1024, dp, 24 bit 1024x768, sp, 24bit 1920x1200, dp, 24bit 800x480, sp, 18bit 1280x800, sp, 18bit 1366x768, sp, 24bit 1440x900, dp, 18bit 1680x1050, dp, 24bit 1920x1080, dp, 24bit | Select the LCD panel used by the Internal Graphics Device by selecting the appropriate setup item. The first item is Panel 1, the last item is Panel 16. |
| IGD – Panel Scaling | Auto, Force Scaling, Off | Selects the LCD panel scaling option used by the Internal Graphics Device. 1. Auto 2. Force Scaling 3. Off |

| Feature | Options | Description |
|----------------------------|---|---|
| IGD – Backlight Brightness | 0%, 10%, 20%, 30%, 40%, 50%, 60%, 70%, 80%, 90%, 100% | Select the starting brightness for the LVDS backlight signal. Note: some backlight inverters use an inverted level for brightness control – please check the inverter spec. for the display panel |
| DVMT 3.0 Mode | Fixed, DVMT, Combo | Select the configuration of DVMT 3.0 Graphics Memory that Driver will allocate for use by the Internal Graphics Device. 1. Fixed 2. DVMT 3. Combo |
| Pre-Allocated Memory Size | 1 MB, 8 MB | Select the amount of Pre-Allocated Graphics Memory for use by the Internal Graphics Device. |
| Total graphics Memory | 64MB, 128 MB, MaxDVMT | Select the amount of Total Graphics Memory Pre-Allocated + Fixed + DVMT for use by the Internal for use by the Internal Graphics Device. |
| DVMT Graphics Memory | N/A | Displays the Memory size of the Video device. |
| Onboard EDID EEPROM | Disabled, Enabled | Enables or disables the Onboard EEPROM for EDID. |

4.2.3.5 ICH Control Sub Menu

| Feature | Options | Description |
|--------------------------------|----------------|---|
| PCI Express Control Submenu | Submenu. | Configure PCI Express Control |
| PCI Control Submenu | Submenu | Configure PCI Control |
| ICH USB Contol Submenu | Submenu | Configure ICH USB Control |
| Azalia – Device 27, Function 0 | Disabled, Auto | Control Detection of the Azalia Device. Disabled = Azalia will be unconditionally disabled, regardless of presence. Auto = Azalia will be enabled if present, disabled otherwise. |

| Feature | Options | Description |
|-------------------------------|----------------------|---|
| AC97A – Device 30, Function 2 | Disabled, Auto | <p>Control Detection of the AC97 Audio Device.</p> <p>Disabled = AC97 Audio will be unconditionally disabled, regardless of presence.</p> <p>Auto = AC97 Audio will be enabled if present, disabled otherwise.</p> |
| AC97M – Device 30, Function 3 | Disabled, Auto | <p>Control Detection of the AC97 Modem Device.</p> <p>Disabled = AC97 Modem will be unconditionally disabled, regardless of presence.</p> <p>Auto = AC97 Modem will be enabled if present, disabled otherwise.</p> |
| AC97 Modem PNE Enable | Disabled, Enabled | Control the ability to wake the System from an AC97 Modem Device |
| SATA – Device 31, Function 2 | Compatible, Enhanced | <p>Compatible: SATA Drive = Primary on SATA Controller, in Legacy Mode. PATA Drive = Secondary on SATA Controller, in Legacy Mode</p> <p>Enhanced: SATA Drive = Primary on SATA Controller, in Native Mode. PATA Drive = Primary on PATA Controller, in Legacy Mode</p> |
| AHCI Configuration | Disabled, Enabled | Enhanced AHCI: WinXP-SP1+IAA driver supports AHCI mode. |
| Disable Vacant Ports | Disabled, Enabled | Controls automatic disabling if vacant SATA ports. |
| On-board LAN | Disabled, Enabled | <p>Setting item to “Disabled” will remove the LAN from PCI Config Space.</p> <p>Setting item to “Enabled” will allow the LAN to operate correctly.</p> |
| PXE OPROM | Disabled, Enabled | Enable PXE Option ROM. |

| Feature | Options | Description |
|-----------------------|-------------------|---|
| Pop Up Mode Enable | Disabled, Enabled | Select the proper mode: If disabled, bus master traffic is a break event and it will return from C3/C4 to C0 based on break events. If enabled, ICH will observe a bus master request and it will take the system from a C3/C4 state to a C2 state and auto enable bus masters. |
| Pop Down Mode Enable | Disabled, Enabled | Should be enabled only if Pop up is enabled: If disabled, ICH will NOT attempt to automatically return. If enabled, ICH will observe a NO bus master request and it can return to a previous C3 or C4 state. |
| DMI Link ASPM Support | Enabled, Disabled | Control ASPM support for DMI link between GMCH and ICH. |

4.2.3.5.1 PCI Express Control Sub-Menu

| Feature | Options | Description |
|-----------------------------|-------------------------|---|
| PCI Express – Root Port 1-6 | Disabled, Enabled, Auto | Control PCI Express Port via this setup option. Disabled = Port always Disabled. Auto = Only enable if card found. Note that if Root Port 1 is disabled Root Ports 2-6 will be disabled as well. |
| Root Port ASPM Support | Disabled, Auto | Control ASPM support for all the enabled Root Ports. Auto = will set APMC to the highest common supported ASPM between the Port and Endpoint. |
| ASPM Latency Checking | Disabled, Enabled | Disabled: ASPM latencies are ignored when enabling ASPM. Enabled: Enables ASPM latency checking when enabling ASPM. |

4.2.3.5.2 PCI Control Sub-Menu

| Feature | Options | Description |
|----------------|--|--|
| PCI IRQ line 1 | Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12 | Select which Interrupt should be assigned to this PCI Irq. Devices :IGD, PEG Port, PCI Slot 1, PCIe Port1, PCIe Port5 |
| PCI IRQ line 2 | Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12 | Select which Interrupt should be assigned to this PCI Irq. Devices: PCI Slot 2, PCIe Slot2, PCIe Port 6 |
| PCI IRQ line 3 | Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12 | Select which Interrupt should be assigned to this PCI Irq. Devices: PCI Slot 3, PCIe Port 3 |
| PCI IRQ line 4 | Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12 | Select which Interrupt should be assigned to this PCI Irq. Devices: PCI Slot 4, PCIe Port 4 |
| PCI IRQ line 5 | Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12 | Select which Interrupt should be assigned to this PCI Irq. Devices: UHCI Controller 1 |
| PCI IRQ line 6 | Auto Select, 3, 4, 5, 6, 7, 10, 11, 12 | Select which Interrupt should be assigned to this PCI Irq. Devices: UHCI Controller 2, PATA/SATA Controller, SMBus |
| PCI IRQ line 7 | Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12 | Select which Interrupt should be assigned to this PCI Irq. Devices: UHCI Controller 3, HD Audio or AC97 Audio |
| PCI IRQ line 8 | Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12 | Select which Interrupt should be assigned to this PCI Irq. Devices: UHCI Controller 4, EHCI Controller, AC97 Modem |

4.2.3.5.3 ICH USB Control Sub-Menu

| Feature | Options | Description |
|----------------------|--|--|
| USB 1.1 Controllers | Enable 1, Enable 2, Enable 3, Enable 4 | Select the number of enabled USB1.1 Controllers. |
| USB 2.0 Controller | Disabled, Enabled | Control USB 2.0 functionality through this Setup Item. |
| Boot from USB Port 1 | Enable, Disable | Set the boot capability for this usb port When set to disabled, mass storage devices will not be able to boot from this port. |
| Boot from USB Port 2 | Enable, Disable | Set the boot capability for this usb port When set to disabled, mass storage devices will not be able to boot from this port. |
| Boot from USB Port 3 | Enable, Disable | Set the boot capability for this usb port When set to disabled, mass storage devices will not be able to boot from this port. |
| Boot from USB Port 4 | Enable, Disable | Set the boot capability for this usb port When set to disabled, mass storage devices will not be able to boot from this port. |
| Boot from USB Port 5 | Enable, Disable | Set the boot capability for this usb port When set to disabled, mass storage devices will not be able to boot from this port. |
| Boot from USB Port 6 | Enable, Disable | Set the boot capability for this usb port When set to disabled, mass storage devices will not be able to boot from this port. |
| Boot from USB Port 7 | Enable, Disable | Set the boot capability for this usb port When set to disabled, mass storage devices will not be able to boot from this port. |
| Boot from USB Port 8 | Enable, Disable | Set the boot capability for this usb port When set to disabled, mass storage devices will not be able to boot from this port. |

4.2.3.6 ACPI Control Sub-Menu

| Feature | Options | Description |
|--|--|--|
| Enable ACPI | No, Yes | En/Disable ACPI BIOS (Advanced Configuration and Power Interface) |
| Disable ACPI _Sx | None, S1, S2, S3, S5 | Select one of the ACPI power states: S1, S2, or S3. If selected, the corresponding power state will be disabled. |
| FACP – RTC S4 Flag Value | Disabled, Enabled | Valid only for ACPI Control the value for the RTC S4 flag in the FACP Table |
| FACP – PM Timer Flag Value | Disabled, Enabled | Valid only for ACPI Controls the timer used by the OS through the FACP Tables Flags. This is now possible with WINXP SP2 and beyond. |
| HPET Support | Disabled, Enabled | This field is valid only in the WindowsXP OS. Control the High Performance Event Timer through this setup option when enabled. The HPET Table will then be pointed to by the RSDT and the proper enable bits will be set. |
| HPET Base Address | 0xFED00000, 0xFED01000, 0xFED02000, 0xFED03000 | Select the Base Address for the High Performance Event Timer. |
| Passive Cooling Trip Point | Disabled, 47 C, 55 C, 63 C, 71 C, 79 C, 87 C, 95 C, 103 C, 111 C, 119 C | This value controls the temperature of the ACPI Passive Trip Point – the point in which the OS will begin throttling the CPU. Note: If the DTS is enabled, only values below 97C are valid. |
| Passive TC1 Value, Passive TC2 Value, | 0 - 15 | This value sets the TC1-2 value for the ACPI Passive Cooling Formula. |
| Passive TSP Value | 1 - 15 | This item sets the TSP value for the ACPI Passive Cooling Formula. It represents in tenths of a second how often the OS will read the temperature when Passive Cooling is Enabled. |

| Feature | Options | Description |
|---------------------|--|--|
| Critical Trip Point | POR, 47 C, 55 C, 63 C, 71 C, 79 C, 87 C, 95 C, 103 C, 111 C, 119 C, 127 C | This value controls the temperature of the ACPI Critical Trip Point – the point in which the OS will shut the system off. Notes: (1)100C is POR for all Intels CPUs. (2) If value is > 100C and DTS is enabled, the Out-of-Spec Bit will be used. (3) The EC value will be set to 127 after ACPI initiation. |

4.2.3.7 Clock Control Sub-Menu

| Feature | Options | Description |
|---------------------------|--|--|
| CK-505 Clock Chip | Program | Control Programming of the CK-505 Clock Chip. Program = TBD. |
| PLL1 Spread Spectrum Mode | Off, Down Spread, Center Spread | Programming of PLL1 Spread Spectrum Clock Off : PLL1 Spektrum is disabled Down Spread = 0.5% Center Spread = 0.25% |
| PLL3 Spread Spectrum | Off, Software | Programming of PLL3 Spread Spectrum Clock Off : PLL1 Spektrum is disabled Software = Spread Spectrum is Bios Controlled with following supported ranges : Down Spread: 0.5% - 2% Center Spread: 0.25% - 0.5% |
| Spread Percentage | Down 0.5%, Down 1%, Down 1.5%, Center 0.25%, Center 0.5% | If controlled by Software, select Percentage of PLL3 Spread Spectrum |

4.2.3.8 I/O Device Configuration Menu

| Feature | Options | Description |
|------------------|-------------------------|--|
| Serial Port A | Disabled, Enabled, Auto | Disabled = Disabled the device Enabled = User configuration Auto = BIOS or OS chooses configuration |
| Base I/O address | 3F8, 2F8, 3E8, 2E8 | Set the base I/O address for Serial |

| Feature | Options | Description |
|------------------|----------------------------------|--|
| | | Port A. |
| Interrupt | 3, 4 | Set the interrupt for Serial Port A. |
| Serial Port B | Disabled, Enabled, Auto | Disabled = Disabled the device Enabled = User configuration Auto = BIOS or OS chooses configuration |
| Mode | Normal, IR, ASK-IR | Set the mode for Serial Port B (wired / infrared). |
| Base I/O address | 3F8, 2F8, 3E8, 2E8 | Set the base I/O address for Serial Port B. |
| Interrupt | 3, 4 | Set the interrupt for Serial Port B. |
| Parallel Port | Disabled, Enabled, Auto | Disabled = Disabled the device Enabled = User configuration Auto = BIOS or OS chooses configuration |
| Mode | Output only, Bi-directional, ECP | Set the mode for Parallel Port. |
| Base I/O address | 378, 278, 3BC | Set the base I/O address for Parallel Port. |
| Interrupt | 5, 7 | Set the interrupt for Parallel Port. |
| DMA channel | 1, 3 | Set the DMA channel for Parallel Port (only available if mode was set to ECP). |

Warning: If you choose the same I/O address or Interrupt for more than one port, the menu displays an asterisk (*) at the conflicting setting.

4.2.3.9 Watchdog Options

| Feature | Options | Description |
|------------------------|--|--|
| Watchdog delay | 1 second, 5 seconds, 10 seconds, 30 seconds 1 minute , 5 minutes, 10 minutes, 30 minutes | After watchdog is activated, it waits selected delay time before it starts counting the timeout period. |
| Watchdog timeout | 0.4 second, 1 second, 5 seconds, 10 seconds, 30 seconds, 1 minute , 5 minutes, 10 minutes | Select the maximum watchdog trigger period. If the watchdog will not be triggered during selected period, system reset will be generated. |
| Watchdog start on boot | No, Yes | Select if the watchdog should be started at the end of POST. |

4.2.4 The Security Menu

| Feature | Options | Description |
|-------------------------|---|---|
| Supervisor Password Is | Displays Supervisor Password Is | Displays the current status of the Supervisor password ("Clear" or "Set") |
| User Password Is | Displays User Password Is | Displays the current status of the User password ("Clear" or "Set") |
| Set Supervisor Password | Press return to enter supervisor password | Supervisor Password controls access to the setup utility. |
| Set User Password | Press return to enter user password | User Password controls access to the system at boot. |
| Password on boot | Disabled, Enabled | Enables password entry on boot |
| TPM Support | Disabled, Enabled | Enable Trusted Platform Module support. |
| Current TPM State | Displays Current TPM State | Displays the current TPM status. |
| Change TPM State | No Change, Enable & Activate, Deactivate & Disable, Clear | Changes TPM state. |

The Power Menu

| Feature | Options | Description |
|---------------------|--------------------|---|
| After Power Failure | Stay Off, Power On | <p>Sets the mode of operation if an AC power loss occurs.</p> <p>Power On will turn the power on as soon as the power supply is back on.</p> <p>Stay Off will keep the power off until the power button is pressed.</p> |
| Hardware Monitor | Submenu | Configure Hardware Monitor |

4.2.5.1 Hardware Monitoring Menu

| Feature | Description |
|--------------------------------------|--|
| CPU Vcore | Displays the current CPU voltage. |
| VRam (V+2.5) ¹⁾ | Displays the current voltage. |
| Vcc (V+3.3) ¹⁾ | Displays the current voltage. |
| VIN1 (V+5.0) ¹⁾ | Displays the current voltage. |
| VIN2 (V+12.0) | Displays the current voltage. |
| CPU Temperature Sensor | Displays the current CPU temperature. |
| GMCH Temperature Sensor | Displays the current GMCH temperature. |
| Memory Temperature Sensor | Displays the current memory temperature. |
| ICH Temperature Sensor ¹⁾ | Displays the current ICH temperature. |
| FAN 1 speed | Displays the current fan speed. |

1) Only supported with hardware revisions less than V2.0.

4.2.6 The Boot Menu

After you turn on your computer, it will attempt to load the operating system (such as DOS, Windows XP or Linux) from a device listed in the boot priority order. If it cannot find the operating system on that device, it will attempt to load it from the next device in that list. Boot devices (i.e., with access to an operating system) can include: hard drives, floppy drives, CD ROMs, removable devices (e.g. USB sticks), and network cards.

Note: Specifying any device as a boot device on the Boot Menu requires the availability of an operating system on that device.

Selecting "Boot" from the Menu Bar displays the Boot menu, which looks like this:

| Feature | Description |
|---|--|
| Boot priority order: 1: USB KEY: 2: USB FDC: 3: IDE 4: 4: IDE 5: 5: IDE 0: 6: IDE 2: 7: PCI LAN: 8: | Boot priority order for next boot. System tries to boot the first bootable device in this list. Use <+> and <-> to change order. Use <x> to exclude or include device to boot priority list. |
| Exclude from boot order: : IDE 1: : IDE 3: : USB HDD: : USB CDROM: : USB ZIP: : USB LS120: : PCI SCSI: | System does not try to boot a device from this list. |

Pressing the "F10" key during the bios boot phase will bring up the bios boot menu, which will allow you to select a different boot device for the current boot process only. In this boot menu, only devices in the "Boot priority list" will selectable. Devices excluded from boot order will not be shown.

The Exit Menu

The following sections describe each of the options on this menu. Note that <Esc> does not exit this menu. You must select one of the items from the menu or menu bar to exit.

Exit Saving Changes

After making your selections on the Setup menus, always select "Exit Saving Changes". This procedure stores the selections displayed in the menus in CMOS (short for "battery-backed CMOS RAM") a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS.

If you attempt to exit without saving, the program asks if you want to save before exiting. During boot-up, PhoenixBIOS attempts to load the values saved in CMOS. If those values

cause the system boot to fail, reboot and press <F2> to enter Setup. In Setup, you can get the Default Values (as described below) or try to change the selections that caused the boot to fail.

Exit Discarding Changes

Use this option to exit Setup without storing in CMOS any new selections you may have made. The selections previously in effect remain in effect.

Load Setup Defaults

To display the default values for all the Setup menus, select "Load Setup Defaults" from the Main Menu.

If, during boot-up, the BIOS program detects a problem in the integrity of values stored in CMOS, it displays these messages:

System CMOS checksum bad - run SETUP Press <F1> to resume, <F2> to Setup

The CMOS values have been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS.

Press <F1> to resume the boot or <F2> to run Setup with the ROM default values already loaded into the menus. You can make other changes before saving the values to CMOS.

Discard Changes

If, during a Setup Session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you previously saved to CMOS.

Selecting "Discard Changes" on the Exit menu updates all the selections with their previous values.

Save Changes

Selecting "Save Changes" saves all the selections without exiting Setup. You can return to the other menus if you want to review and change your selections.

4.3 Bios Update

If a System-BIOS update is required please follow these instructions:

- 1.) Create a bootable DOS disk/usb-stick/hdd.
- 2.) Copy PHLASH16.EXE, BIOS.WPH and UPDATE.BAT to this device.
- 3.) Boot the system from this device.
- 4.) Type "update.bat" to update the System BIOS.
- 5.) When the BIOS update has finished, reboot the system.

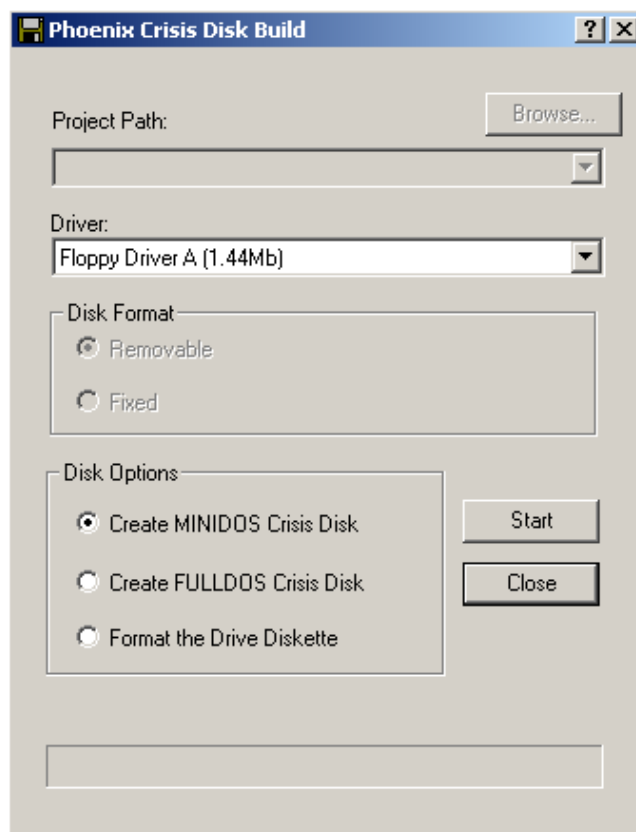
Note: After the system has been updated, the CMOS has been changed to defaults and therefore it is necessary to enter Setup (press F2 at boot time) to configure the system settings.

4.4 Bios Crisis Recovery

Note: Contact your sales for information how to get the CRISDISK.ZIP and an USB recovery dongle.

Please follow these simple steps to create a bootable crisis recovery medium:

Unzip CRISDISK.ZIP and start the windows-based program WINCRIS.EXE on the host system. A window will pop up as shown below:



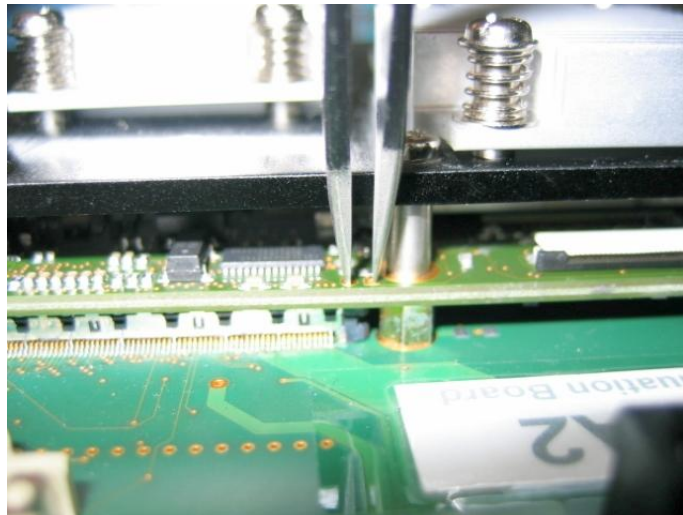
In the drop-down box, either select "Floppy Drive A" to create a recovery disk, or select "Removable Disk 0 (xxxMb)" to create a recovery usb stick. Disk options should be left at "Create MINIDOS Crisis Disk".

Press the start button to generate the selected crisis recovery medium.

There are two possibilities to force the target system into crisis recovery mode: either by USB crisis recovery dongle or by crisis recovery jumper.

With the dongle, you just have to plug it into a free USB port before switching the system on. Please make sure that you use different USB controllers for USB dongle and USB crisis recovery medium. After power up, crisis recovery mode should automatically start.

The crisis recovery jumper is located next to Com Express Board Connector the (see picture below). You have to short the two pins before applying power to the board. As soon as crisis recovery is started, you can remove the jumper.



The programming process is signalled by short beeps and terminated after successful programming with one long beep. After that, the system is automatically rebooted.

Important Notes:

USB recovery dongle and USB crisis recovery device must not be plugged to the same USB controller.

Crisis recovery may take up to 5 minutes

A long beep indicated successful recovery

Crisis recovery does not include the bootblock.

4.5 *Diagnostics Postcodes*

Postcodes can be seen on a special Postcode display, either on the MSC mainboard or on an external Postcode PCI card. There is an item in the bios setup to select the bus that should get the postcode data: either PCI (for external cards) or LPC (for onboard displays).

If a postcode display has only 2 digits, only the lower byte of word-value postcodes will be shown.

4.5.1 **Bootblock Bios Postcodes**

| Code | Bootblock Task Description |
|-------------|--|
| BBH | Bootblock Early Init after Reset |
| 80h | Chipset Init |
| 81h | Bridge Init |
| 82h | CPU Init |
| 83h | System Timer Init |
| 84h | System I/O Init |
| 85h | Check forced Recovery Boot, CMOS & CMOS Backup Clear |
| 86h | Check BIOS Checksum |
| 87h | Goto BIOS, start early BIOS initializations |
| 88h | Init Multi Processor |
| 89h | Set Huge Segment |
| 8Ah | OEM Initializations |
| 8Bh | Init Interrupt and DMA Controller |
| 8Ch | Init Memory Type |
| 8Dh | Init Memory Size |
| 8Eh | Shadow Boot Block |
| 8Fh | Init SMM |
| 90h | System Memory Test |
| 91h | Init Interrupt Vectors |
| 92h | Init Realtime Clock |
| 93h | Init Standard Video |
| 94h | Init Beeper |
| 95h | Initialize USB Controller |
| 95h | Init Boot |
| 96h | Clear Huge Segment |
| 97h | Boot OS |
| 99h | Init Security |

4.5.2 System Bios Postcodes

| Code | Beeps | POST Task Description |
|------|---------|---|
| 04h | | Get CPU type |
| 03h | | Disable Non-Maskable Interrupt (NMI) |
| 06h | | Initialize system hardware |
| 07h | | Disable shadow and execute code from the ROM. |
| 08h | | Initialize chipset with initial POST values |
| 09h | | Set IN POST flag |
| 0Ah | | Initialize CPU registers |
| 0Bh | | Enable CPU cache |
| 0Ch | | Initialize caches to initial POST values |
| 0Eh | | Initialize I/O component |
| 0Fh | | Initialize fixed disk drives |
| 10h | | Initialize Power Management |
| 11h | | Load alternate registers with initial POST values |
| 12h | | Restore CPU control word during warm boot |
| 13h | | Initialize PCI Bus Mastering devices |
| 14h | | Initialize keyboard controller |
| 16h | 1-2-2-3 | BIOS ROM checksum |
| 17h | | Initialize cache before memory Autosize |
| 18h | | 8254 timer initialization |
| 1Ah | | 8237 DMA controller initialization |
| 1Ch | | Reset Programmable Interrupt Controller |
| 20h | 1-3-1-1 | Test DRAM refresh |
| 22h | 1-3-1-3 | Test 8742 Keyboard Controller |
| 24h | | Set ES segment register to 4 GB |
| 28h | | Autosize DRAM |
| 29h | | Initialize POST Memory Manager |
| 2Ah | | Clear 512 kB Base RAM |
| 2Ch | 1-3-4-1 | RAM Address test |
| 2Eh | 1-3-4-3 | Base RAM Test |
| 2Fh | | Enable cache before system BIOS shadow |
| 32h | | Compute CPU clock speed in MHz |
| 33h | | Initialize Phoenix Dispatch Manager |
| 36h | | Warm start shut down |
| 38h | | Shadow system BIOS ROM |
| 3Ah | | Autosize cache |
| 3Ch | | Advanced configuration of chipset registers |
| 3Dh | | Load alternate registers with CMOS values |
| 41h | | Initialize RomPilot |
| 42h | | Initialize interrupt vectors |
| 45h | | POST device initialization |
| 46h | 2-1-2-3 | Check ROM copyright notice |
| 47h | | Initialize I20 support |
| 48h | | Check video configuration against CMOS |
| 49h | | Initialize PCI bus and devices |
| 4Ah | | Initialize all video adapters in system |
| 4Bh | | QuietBoot start (optional) |
| 4Ch | | Shadow video BIOS ROM |
| 4Eh | | Display BIOS copyright notice |
| 4Fh | | Initialize MultiBoot |
| 50h | | Display CPU type and speed |

| Code | Beeps | POST Task Description |
|------|---------|---|
| 51h | | Initialize EISA board |
| 52h | | Test keyboard |
| 54h | | Set key click if enabled |
| 55h | | Configure USB devices |
| 58h | 2-2-3-1 | Test for unexpected interrupts |
| 59h | | Initialize POST display service |
| 5Ah | | Display prompt "Press F2 to enter SETUP" |
| 5Bh | | Disable CPU cache |
| 5Ch | | Conventional memory test |
| 60h | | Extended memory test |
| 62h | | Address Test on Extended Memory |
| 64h | | Jump to UserPatch1 |
| 66h | | Configure advanced cache registers |
| 67h | | CPU feature, MP, and APIC initialization |
| 68h | | Enable external and CPU caches |
| 69h | | Setup System Management Mode (SMM) area |
| 6Ah | | Display external L2 cache size |
| 6Bh | | Load custom defaults (optional) |
| 6Ch | | Display BIOS shadow status |
| 70h | | Display error messages |
| 72h | | Check for configuration errors |
| 76h | | Check for keyboard errors |
| 7Ch | | Set up hardware interrupt vectors |
| 7Dh | | Initialize Intelligent System Monitoring |
| 7Eh | | Initialize coprocessor if present |
| 80h | | Disable onboard Super I/O ports and IRQs |
| 81h | | Late POST device initialisation |
| 82h | | Detect and install external RS232 ports |
| 83h | | Configure non-MCD IDE controllers |
| 84h | | Detect and install external parallel ports |
| 85h | | Initialize PC-compatible PnP ISA devices |
| 86h | | Re-initialize onboard I/O ports. |
| 87h | | Configure Motheboard Configurable Devices (optional) |
| 88h | | Initialize BIOS Data Area |
| 89h | | Enable Non-Maskable Interrupts (NMIs) |
| 8Ah | | Initialize Extended BIOS Data Area |
| 8Bh | | Test and initialize PS/2 mouse |
| 8Ch | | Initialize floppy controller |
| 8Fh | | Determine number of ATA drives (optional) |
| 90h | | Initialize hard-disk controllers |
| 91h | | Program timing registers according to PIO modes |
| 92h | | Jump to UserPatch2 |
| 93h | | Build MPTABLE for multi-processor boards |
| 95h | | Install CD ROM for boot |
| 96h | | Clear huge ES segment register |
| 97h | | Fixup Multi Processor table |
| 98h | 1-2 | Enable PCI devices and ROM Scan One long, two short beeps on checksum failure |
| 99h | | Check for SMART Drive |
| 9Ah | | Shadow option ROMs |
| 9Ch | | Set up Power Management |
| 9Dh | | Initialize security engine (optional) |
| 9Eh | | Enable hardware interrupts |
| 9Fh | | Determine number of ATA and SCSI drives |

| Code | Beeps | POST Task Description |
|-------------|--------------|---|
| A0h | | Set time of day |
| A2h | | Check key lock |
| A4h | | Initialize typematic rate |
| A8h | | Erase F2 prompt |
| AAh | | Scan for F2 key stroke |
| ACh | | Enter SETUP |
| A Eh | | Clear Boot flag |
| B0h | | Check for errors |
| B1h | | Inform RomPilot about the end of POST. |
| B2h | | POST done - prepare to boot operating system |
| B3h | | store enhanced CMOS values in non-volatile area |
| B4h | | 1 One short beep before boot |
| B5h | | Terminate QuietBoot (optional) |
| B6h | | Check password (optional) |
| B7h | | Initialize ACPI BIOS |
| B9h | | Prepare Boot |
| BAh | | Initialize DMI parameters |
| BCh | | Clear parity checkers |
| BDh | | Display MultiBoot menu |
| BEh | | Clear screen (optional) |
| BFh | | Check virus and backup reminders |
| C0h | | Try to boot with INT 19 |
| C1h | | Initialize POST PEM Error Manager |
| C2h | | Initialize PEM error logging |
| C3h | | Initialize error PEM display function |
| C4h | | Initialize PEM system error handler |
| C5h | | PnPnd dual CMOS (optional) |
| C6h | | Initialize note dock (optional) |
| C7h | | Initialize note dock late |
| C8h | | Force check (optional) |
| C9h | | Extended checksum (optional) |
| CAh | | Redirect Int 15h to enable remote keyboard |
| CBh | | Redirect Int 13h to Memory Technologies |
| CCh | | Redirect Int 10h to enable remote serial video |
| CDh | | Remap I/O and memory for PCMCIA |
| CEh | | Initialize digitizer and display message |
| D2h | | Unknown interrupt or exception |

4.5.3 Memory Detection Postcodes

| Code | Calistoga Memory Detection |
|-------|---|
| FFA0h | Start memory detection |
| FF01h | Enable MCHBAR |
| FF02h | Check for DRAM initialisation interrupt and reset fail |
| FF03h | Verify all DIMMs are DDR2 and unbuffered |
| FF04h | Detect an improper warm reset and handle |
| FF05h | Detect if ECC SO-DIMMs are present in the system |
| FF06h | Verify all DIMMs are single or double sided and not asymmetric |
| FF07h | Verify all DIMMs are x8 or x16 width |
| FF08h | Find a common CAS latency between the DIMMS and the MCH |
| FF09h | Determine the memory frequency and CAS latency to program |
| FF10h | Determine the smallest common TRAS for all DIMMs |
| FF11h | Determine the smallest common TRP for all DIMMs |
| FF12h | Determine the smallest common TRCD for all DIMMs |
| FF13h | Determine the smallest refresh period for all DIMMs |
| FF14h | Verify burst length of 8 is supported by all DIMMs |
| FF15h | Determine the smallest tWR supported by all DIMMs |
| FF16h | Determine DIMM size parameters |
| FF17h | Program Graphics frequency and PLL settings |
| FF18h | Program system memory frequency |
| FF19h | Determine and set the mode of operation for the memory channels |
| FF20h | Program clock crossing registers |
| FF21h | Disable Fast Dispatch |
| FF22h | Program the DRAM Row Attributes and DRAM Row Boundary registers |
| FF23h | Program the DRAM Bank Architecture register |
| FF24h | Program the DRAM Timing & and DRAM Control registers |
| FF25h | Program ODT |
| FF26h | Perform steps required before memory init |
| FF27h | Program the receive enable reference timing control register Program the DLL Timing Control Registers , RCOMP settings |
| FF28h | Enable DRAM Channel I/O Buffers |
| FF29h | Enable all clocks on populated rows |
| FF30h | Perform JEDEC memory initialization for all memory rows |
| FF31h | Program PM Settings |
| FF32h | Perform additional steps required after memory init |
| FF33h | Program DRAM throttling and throttling event registers |
| FF34h | Setup DRAM control register for normal operation and enable |
| FF35h | Setup DRAM control register for normal operation and enable |
| FF36h | Enable RCOMP |
| FF37h | Clear DRAM initialization bit in the ICH |

4.5.4 ACPI Postcodes

| Code | ACPI Codes |
|------|------------------------------|
| 03h | Enter Suspend State S3 |
| 04h | Enter Hibernate State S4 |
| 05h | Enter Softoff State S5 |
| ABh | Enter Wakeup from Powerstate |
| CDh | End Wakeup from Powerstate |